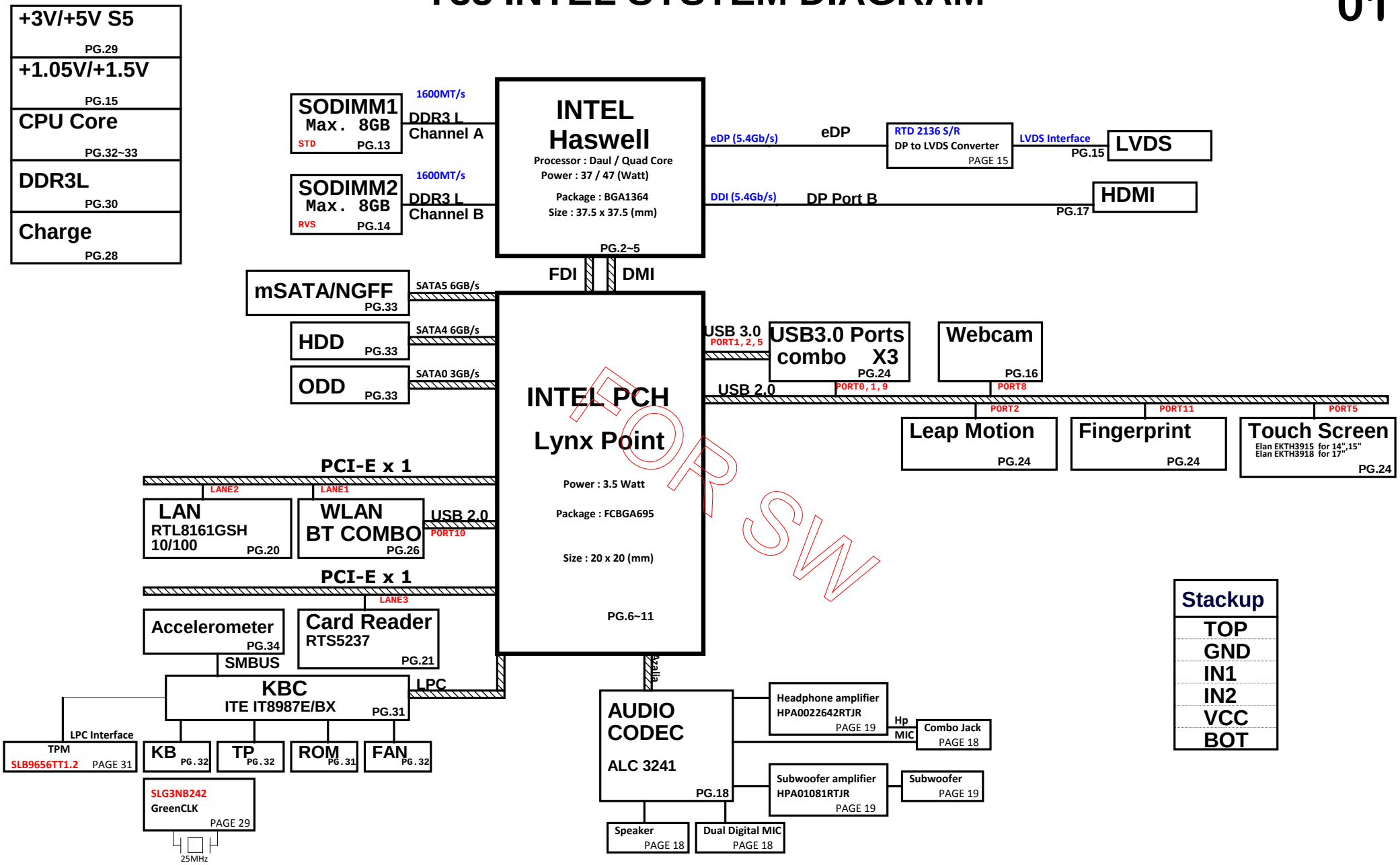
Y33 INTEL SYSTEM DIAGRAM

01



NB5	PROJECT : Y19C Quanta Computer Inc.
Size: Custom	Document Number: BLOCK DIAGRAM
Rev	2A
Date: Wednesday, February 19, 2014	Sheet 1 of 34

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Haswell Processor (DMI,PEG,FDI)

Haswell Processor (CLK,MISC,JTAG)

02

U28A HASWELL_BGA_E

DMI: DMI_RXN0 AB2, DMI_RXN1 AB3, DMI_RXN2 AC3, DMI_RXN3 AC1 [7]
DMI_TXP0 AB1, DMI_TXP1 AB4, DMI_TXP2 AC4, DMI_TXP3 AC2 [7]
DMI_TXN0 AF2, DMI_TXN1 AG4, DMI_TXN2 AG2, DMI_TXN3 [7]
DMI_RXP0 AF1, DMI_RXP1 AF3, DMI_RXP2 AG3, DMI_RXP3 AG1 [7]

FDI: FDI_CSYNC F11 [7] FDI_CSYNC — R179 *0_4/S FDI_CSYNC_R
DISP_INT F12 [7] FDI_INT

PEG: PEG_RCOMP AH6 PEG_COMP; PEG_RXN0 E10, PEG_RXN1 C10, PEG_RXN2 B10, PEG_RXN3 E9, PEG_RXN4 D9, PEG_RXN5 B9, PEG_RXN6 L5, PEG_RXN7 L2, PEG_RXN8 M4, PEG_RXN9 L4, PEG_RXN10 M2, PEG_RXN11 V5, PEG_RXN12 V4, PEG_RXN13 V1, PEG_RXN14 Y3, PEG_RXN15 Y2
PEG_RXP0 F10, PEG_RXP1 D10, PEG_RXP2 A10, PEG_RXP3 F9, PEG_RXP4 C9, PEG_RXP5 A9, PEG_RXP6 M5, PEG_RXP7 M3, PEG_RXP8 L3, PEG_RXP9 M1, PEG_RXP10 Y5, PEG_RXP11 V3, PEG_RXP12 V2, PEG_RXP13 Y4, PEG_RXP14 Y1, PEG_RXP15
PEG_TXN0 B6, PEG_TXN1 C5, PEG_TXN2 E6, PEG_TXN3 D4, PEG_TXN4 G4, PEG_TXN5 E3, PEG_TXN6 J5, PEG_TXN7 G3, PEG_TXN8 J3, PEG_TXN9 J2, PEG_TXN10 T6, PEG_TXN11 R6, PEG_TXN12 R2, PEG_TXN13 R4, PEG_TXN14 T4, PEG_TXN15 T1
PEG_TXP0 C6, PEG_TXP1 B5, PEG_TXP2 D6, PEG_TXP3 E4, PEG_TXP4 G5, PEG_TXP5 E2, PEG_TXP6 J6, PEG_TXP7 G2, PEG_TXP8 J4, PEG_TXP9 J1, PEG_TXP10 T5, PEG_TXP11 R5, PEG_TXP12 R1, PEG_TXP13 R3, PEG_TXP14 T3, PEG_TXP15 T2

1 OF 12

FDI_CSYNC & FDI_INT
Trace length < 10000 Mils
Impendance = 50 ohm

H_PECI (50ohm)
Route on microstrip only
Spacing > 18 mils
Trace Length: 15 inch

TP21, TP23 — PROC_DETECT# — C51 PROC_DETECT#

HPECI Ra,Ca need placement close to EC.
[10,27] EC_PECI — R239 43_4 — H_PECI; Ra; C246 *47P/50V_4; Ca

TP_CATERR# — G50 CATERR#

PROCHOT# (50ohm)
Trace Length <11 inches
[27,32] H_PROCHOT# — R172 56.2/F_4 — H_PROCHOT#_R — G51 PECI
C56 47P/50V_4; Cb — **Cb need placment near VR**
E50 PROCHOT#

THERMTRIP# (50ohm)
Trace Length: 1.1~12 inches
[10,27] PM_THRMTRIP#_R — PM_THRMTRIP#_R — D53 THERMTRIP#
Rb need placment near PCH
4/30 CRB 1.0 Add
+1.05VO R474 100/F_4 Rb

PM_SYNC (50ohm)
Trace Length: 1~11.25 inches
[7] PM_SYNC — R526 0_4 — PM_SYNC_R — D52 PM_SYNC

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches
C153 *0.1U/10V_4
[10] H_PWRGOOD — F50 UNCOREPWRGOOD
R183 10K_4

CPU RESET#
[9,20,21,22,26,27] PLTRST# — R533 *1.5K/F_4 — L54 RESET
[10,27] CPU_PLTRST#R — PM_DRAM_PWRGD_R — AP48 SM_DRAMPWROK
R534 *750/F_4
CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches
7/26: DB phase modify

U28B HASWELL_BGA_E — 2 OF 12

MISC: PROC_DETECT#, CATERR#, PECI, PROCHOT#, THERMTRIP#, SM_DRAMPWROK, RESET
THERMAL; PWR MANAGEMENT; JTAG & BPM

CLOCKS: BCLKP AA6 CLK_CPU_BCLKP [9], BCLKN AB6 CLK_CPU_BCLKN [9]
SSC_DPLL_REF_CLKP Y6 CLK_DPLL_SSCLKP [9], SSC_DPLL_REF_CLKN Y6 CLK_DPLL_SSCLKN [9]
DPLL_REF_CLKP AE6 CLK_DPLL_NSCCLKP [9], DPLL_REF_CLKN AC6 CLK_DPLL_NSCCLKN [9]

DDR3: SM_DRAMRST# BE51 DDR3_DRAMRST# [13,14]
SM_RCOMP0 BB51 SM_RCOMP_0 — R215 100/F_4
SM_RCOMP1 BB53 SM_RCOMP_1 — R213 75/F_4
SM_RCOMP2 BB52 SM_RCOMP_2 — R214 100/F_4
SM_RCOMP[0] W:12mils/S:15mils/L: 500mils,
SM_RCOMP[1] W:12mils/S:15mils/L: 500mils,
SM_RCOMP[2] W:12mils/S:15mils/L: 500mils,

Host CLK:
Trace length < 11000 MILS
Trace spacing = 15 ,20 MILS, Impendence 90 ohm

CPU XDP:
PRDY# N53 XDP_PRDY# — TP58
PREQ# N52 XDP_PREQ# — TP34
TCK N54 XDP_TCLK — TP60
TMS M51 XDP_TMS — TP24
TRST# M53 XDP_TRST# — TP57
TDI N49 XDP_TDI_R — TP30
TDO M49 XDP_TDO — TP25
DBR# F53 XDP_DBRST# — R525 *1K_4 — +3V — XDP_DBRST# [7]
BPM#0 R51 XDP_BPM0 — TP26
BPM#1 R50 XDP_BPM1 — TP31
BPM#2 P49 XDP_BPM2 — TP29
BPM#3 N50 XDP_BPM3 — TP32
BPM#4 R49 XDP_BPM4 — TP28
BPM#5 P53 XDP_BPM5 — TP59
BPM#6 U51 XDP_BPM6 — TP27
BPM#7 P51 XDP_BPM7 — TP61

U28J HASWELL_BGA_E — INTEL (R) DDI

DDIB_TXN0 C25 [17] IN_D2#, DDIB_TXN1 A25 [17] IN_D1#, DDIB_TXN2 C24 [17] IN_D0#, DDIB_TXN3 A24 [17] IN_CLK#
DDIB_TXP0 D25 [17] IN_D2, DDIB_TXP1 B25 [17] IN_D1, DDIB_TXP2 D24 [17] IN_D0, DDIB_TXP3 B24 [17] IN_CLK
DPB_LANE0_N, DPB_LANE1_N, DPB_LANE2_N, DPB_LANE3_N
DPB_LANE0_P, DPB_LANE1_P, DPB_LANE2_P, DPB_LANE3_P

DDIC_TXN0 C21, DDIC_TXN1 A21, DDIC_TXN2 C20, DDIC_TXN3 A20
DDIC_TXP0 D21, DDIC_TXP1 B21, DDIC_TXP2 D20, DDIC_TXP3 B20
DDID_TXN0 C17, DDID_TXN1 A17, DDID_TXN2 C16, DDID_TXN3 A16
DDID_TXP0 D17, DDID_TXP1 B17, DDID_TXP2 D16, DDID_TXP3 B16

eDP: EDP_RCOMP AG6 eDP_RCOMP; EDP_DISP_UTIL E12 — *0_4 — R173 — EDP_DISP_UTIL [7,15,16]; EDP_HPD E14 INT_eDP_HPD_Q
EDP_AUXP F14 — INT_eDP_AUXP [15]; EDP_AUXN F15 — INT_eDP_AUXN [15]
EDP_TXP0 D14 — INT_eDP_TXP0 [15]; EDP_TXP1 B12 — INT_eDP_TXP1 [15]
EDP_TXN0 C14 — INT_eDP_TXN0 [15]; EDP_TXN1 A12 — INT_eDP_TXN1 [15]

FDI: FDI_TXN0 C12 — FDI_TXN0 [16]; FDI_TXN1 A14 — FDI_TXN1 [16]; FDI_TXP0 D12 — FDI_TXP0 [16]; FDI_TXP1 B14 — FDI_TXP1 [16]

SM_DRAMPWROK Processor Input.

To change the resistor values in the DRAMPWROK logic to reduce the leakage on VDDPWRGOOD

+3VS5 — R193 100K_4, R192 100K_4
PM_DRAM_PWRGD_C (50ohm)
Trace Length: <1 inches
C164 0.1U/10V_4
[30] 1P35V_PGOOD — U11 74AHC1G09GW — PM_DRAM_PWRGD_R
C168 0.047U/25V_4, D7 *MEK500V-40
+1.35V_CPU — R203 1.8K/F_4 — **DG 498556 -> 1.8K**
R205 3.3K_4, C210 *0.047U/25V_4 — **DG 498556 -> 3.3K**
PM_DRAM_PWRGD (50ohm)
Trace Length: 2~7 inches
PM_DRAM_PWRGD_R (50ohm)
Trace Length: 0.5~1 inches

+VCCIO_OUT [4,32]
+VCCIOA_OUT [4]
+1.05V [4,10,11,24,27,31]
+1.35V_CPU [4,13,14,17,30]
+1.35VSUS [4,13,14,17,30]
+3VS5 [7,8,10,11,26,29,31,34]
+3V [7,8,9,10,11,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27,32,34]

4/30 CRB V1.0 -> 10K
+VCCIO_OUT — R166 10K_4 — INT_eDP_HPD_Q — Q13 2N7002K — R161 100K_4 — EDP_HPD [15,16]

DP & PEG Compensation

+VCCIOA_OUT — R195 24.9/F_4 — eDP_RCOMP
eDP_RCOMP
Trace length < 100 Mils
Trace Width 20 Mils Trace Spacing 25 Mils
+VCCIOA_OUT — R199 24.9/F_4 — PEG_COMP
PEG_RCOMP
Trace length < 400 MILS
Trace width = 12 MILS
Trace spacing = 15 MILS

Processor pull-up (CPU)

H_PROCHOT# R167 62_4, CLK_DPLL_SSCLKP R191 *10K_4, CLK_DPLL_SSCLKN R188 *10K_4 — +VCCIO_OUT
XDP_TDO R186 51_4, XDP_TMS R184 *51_4, XDP_TDI_R R187 *51_4, XDP_PREQ# R190 *51_4, XDP_TCLK R536 51_4, XDP_TRST# R535 51_4 — +1.05V

NB5

PROJECT : Y19C
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 1/5 (PCIE&DMI&FDI)	2A

Date: Wednesday, February 19, 2014 | Sheet 2 of 34

FOR REVIEW

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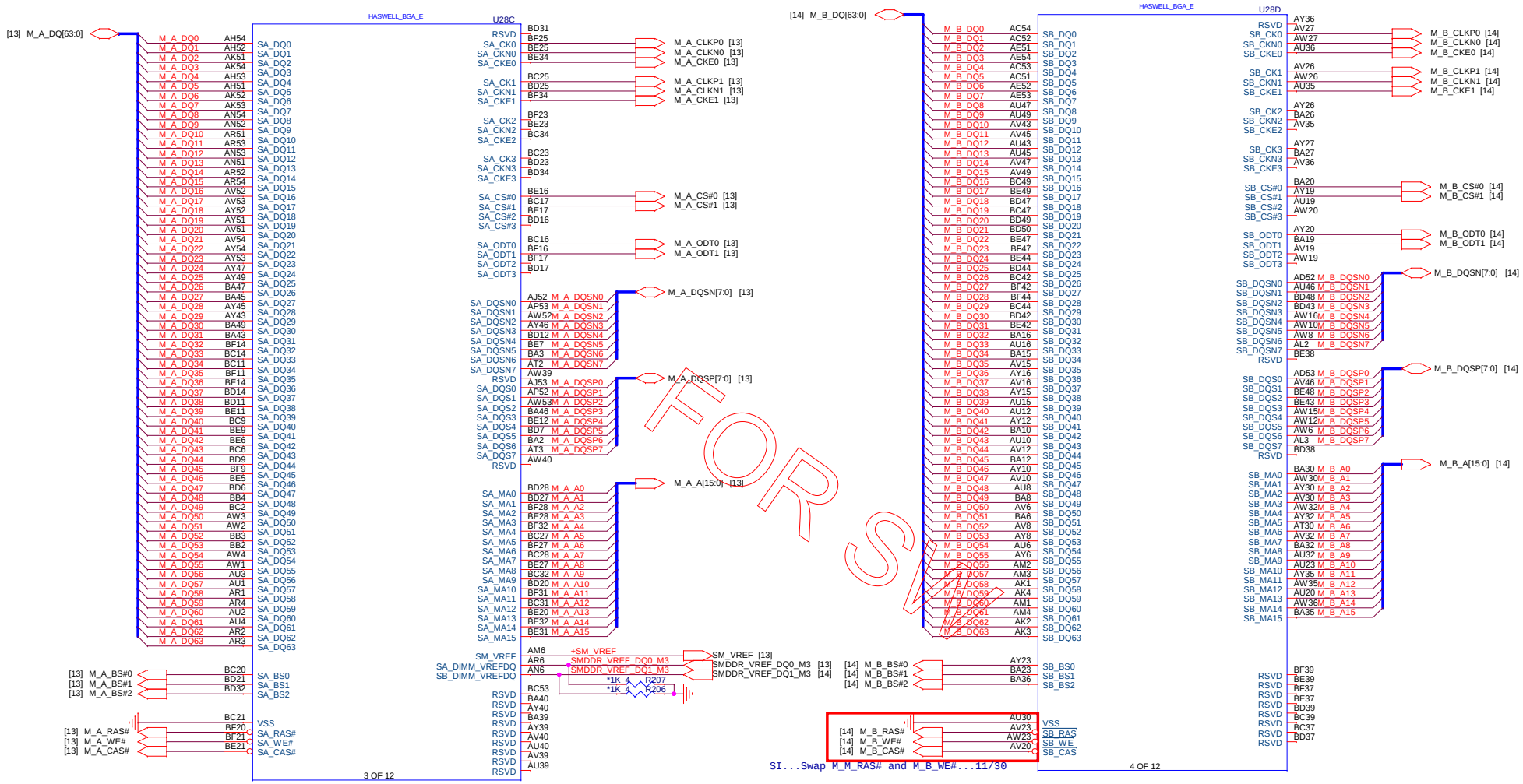
Haswell Processor (DDR3)



RSVD_V10 must be grounded

CPU SM_VREF

PROJECT : Y19C Quanta Computer Inc.	
Size: Custom	Document Number: SNB 2/5 (DDR3 I/F)
Rev: 2A	
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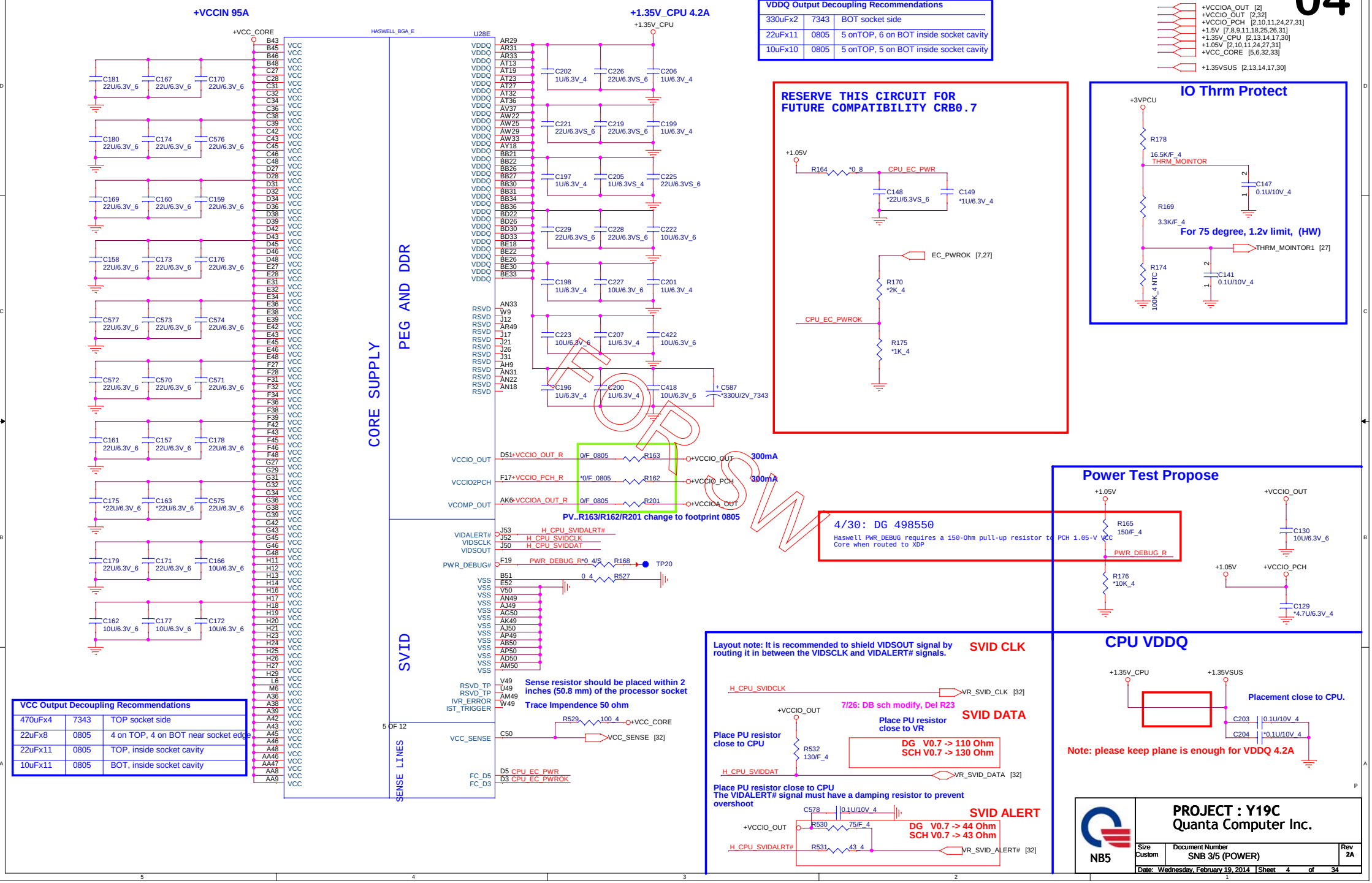
Haswell Processor (POWER)

04



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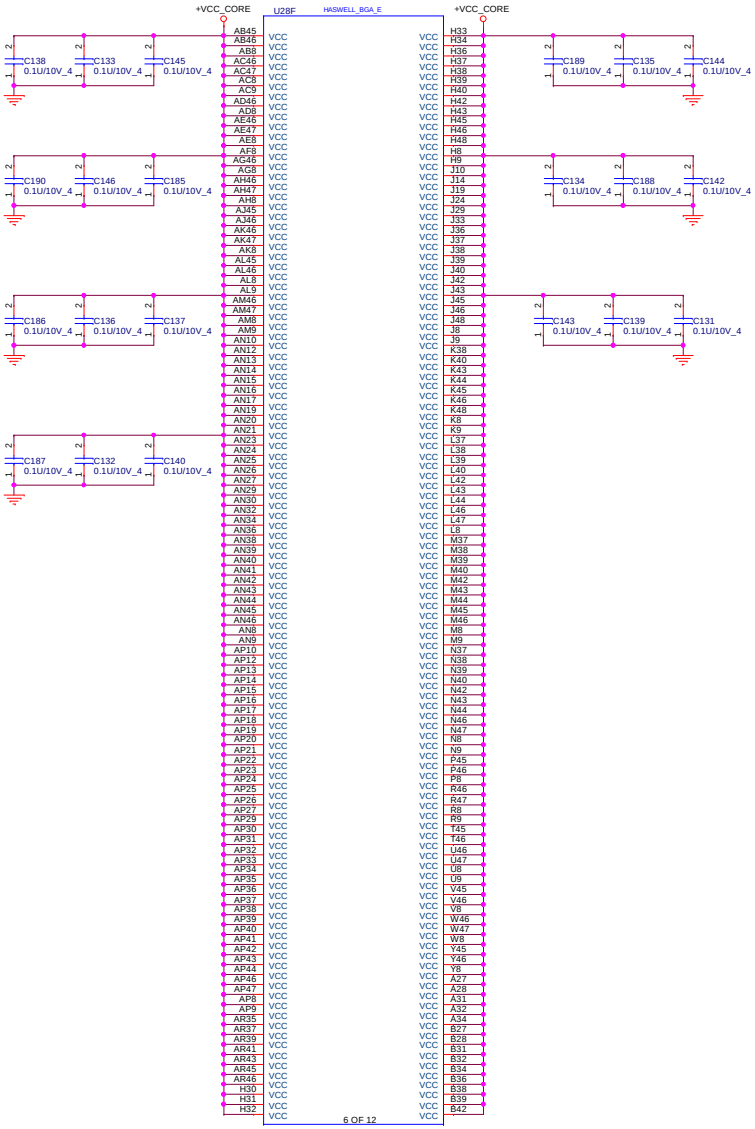

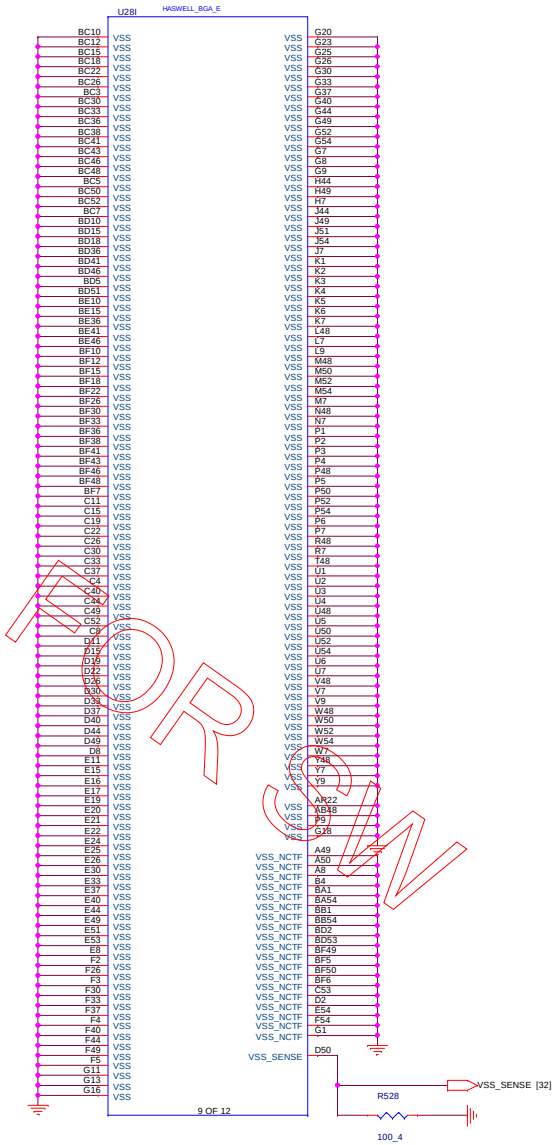

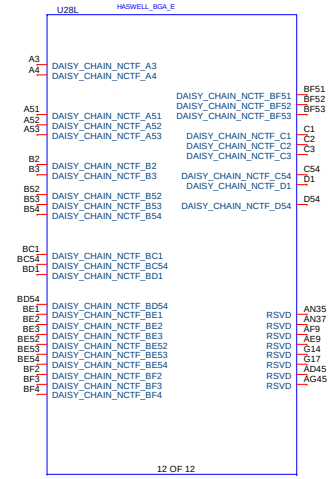

Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket

Trace Impendence 50 ohm

NOT REV

NB5

PROJECT : Y19C
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 4/5 (POWER & GND)	2A

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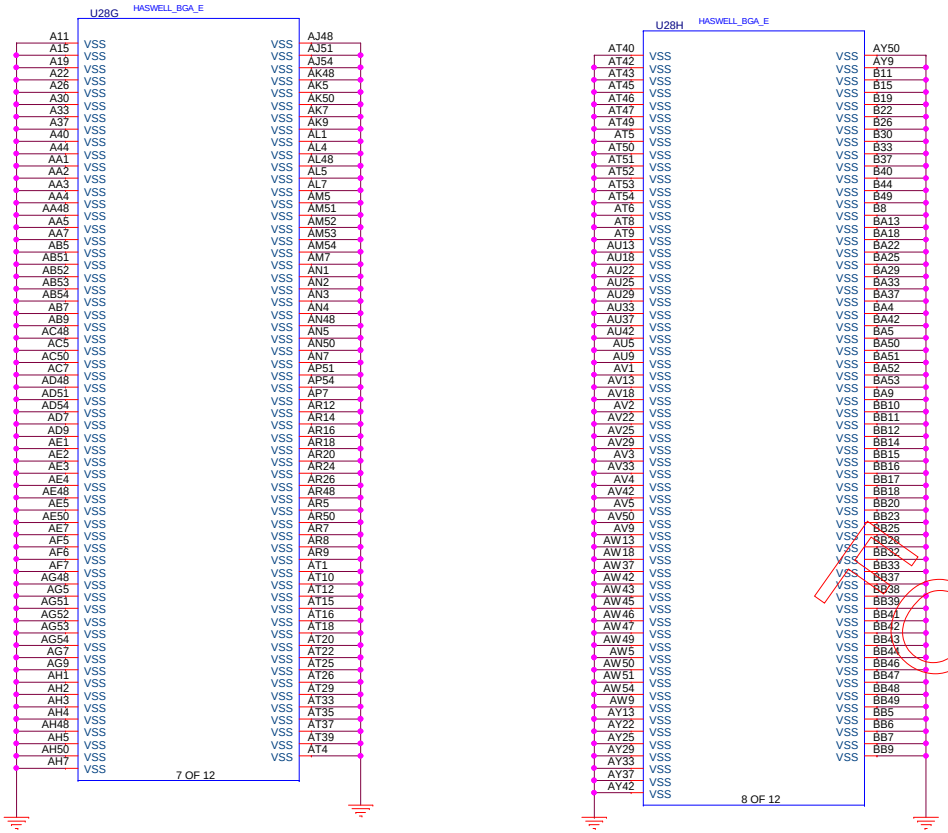
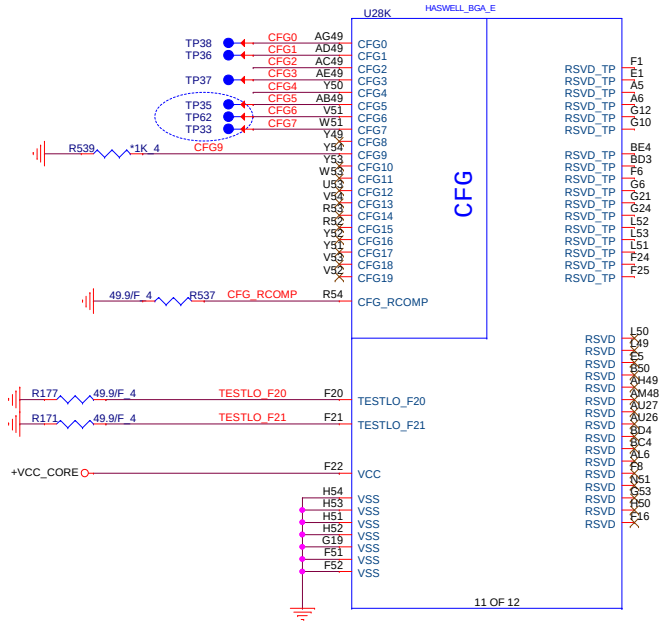
Haswell Processor (GND)



Haswell Processor (RESERVED, CFG)



FOR SW

CFG[3] (PHYSICAL_DEBUG_ENABLED (DFX PRIVACY))

0 Enable; SET DFX ENABLED BIT IN DEBUG

1 , Disable;

CFG3 R200 *1K_4

CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

CFG2 R194 *1K_4

CFG4 R538 1K_4

NB5

PROJECT : Y19C
Quanta Computer Inc.

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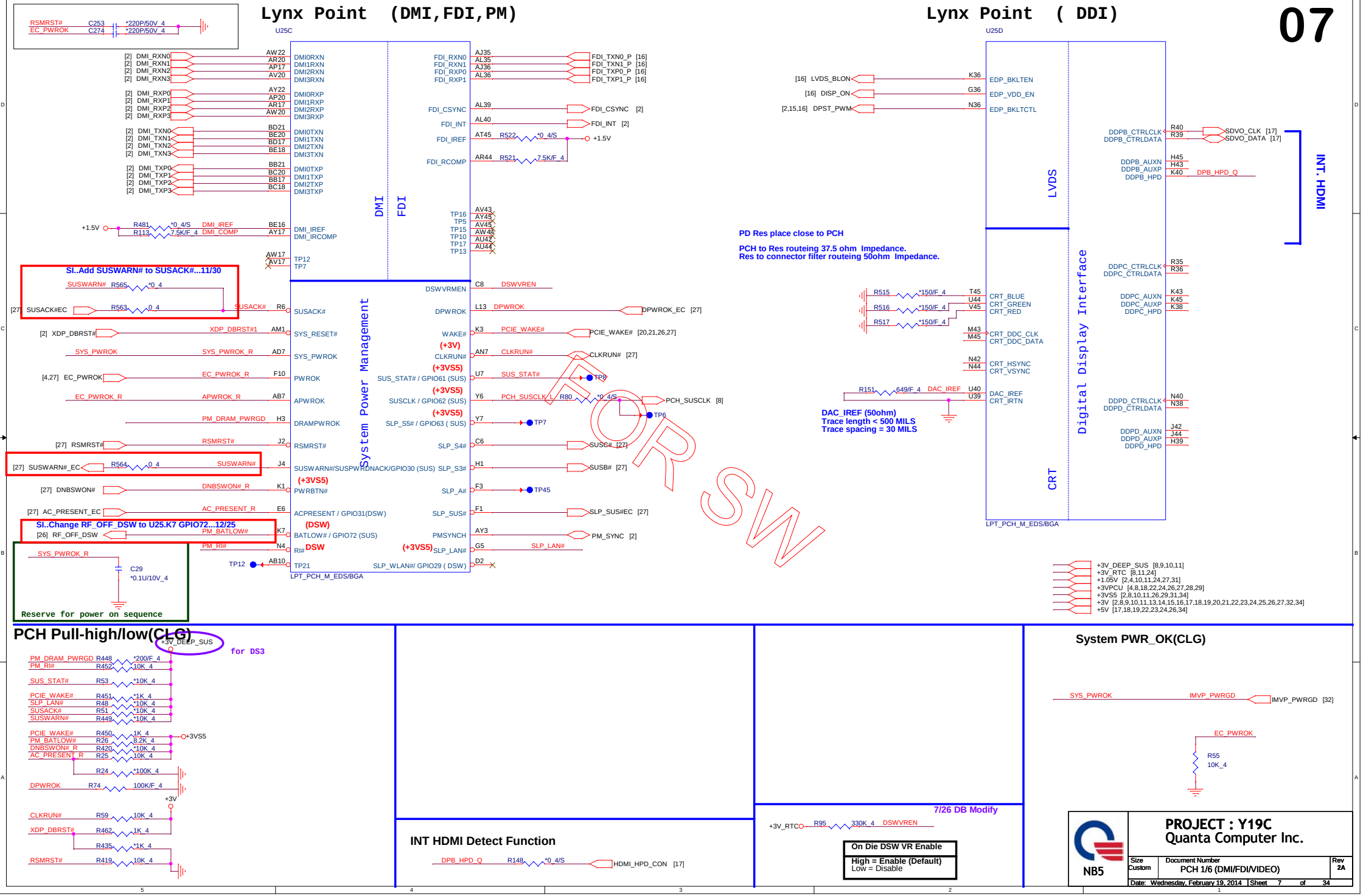
Lynx Point (DMI,FDI,PM)

Lynx Point (DDI)

07



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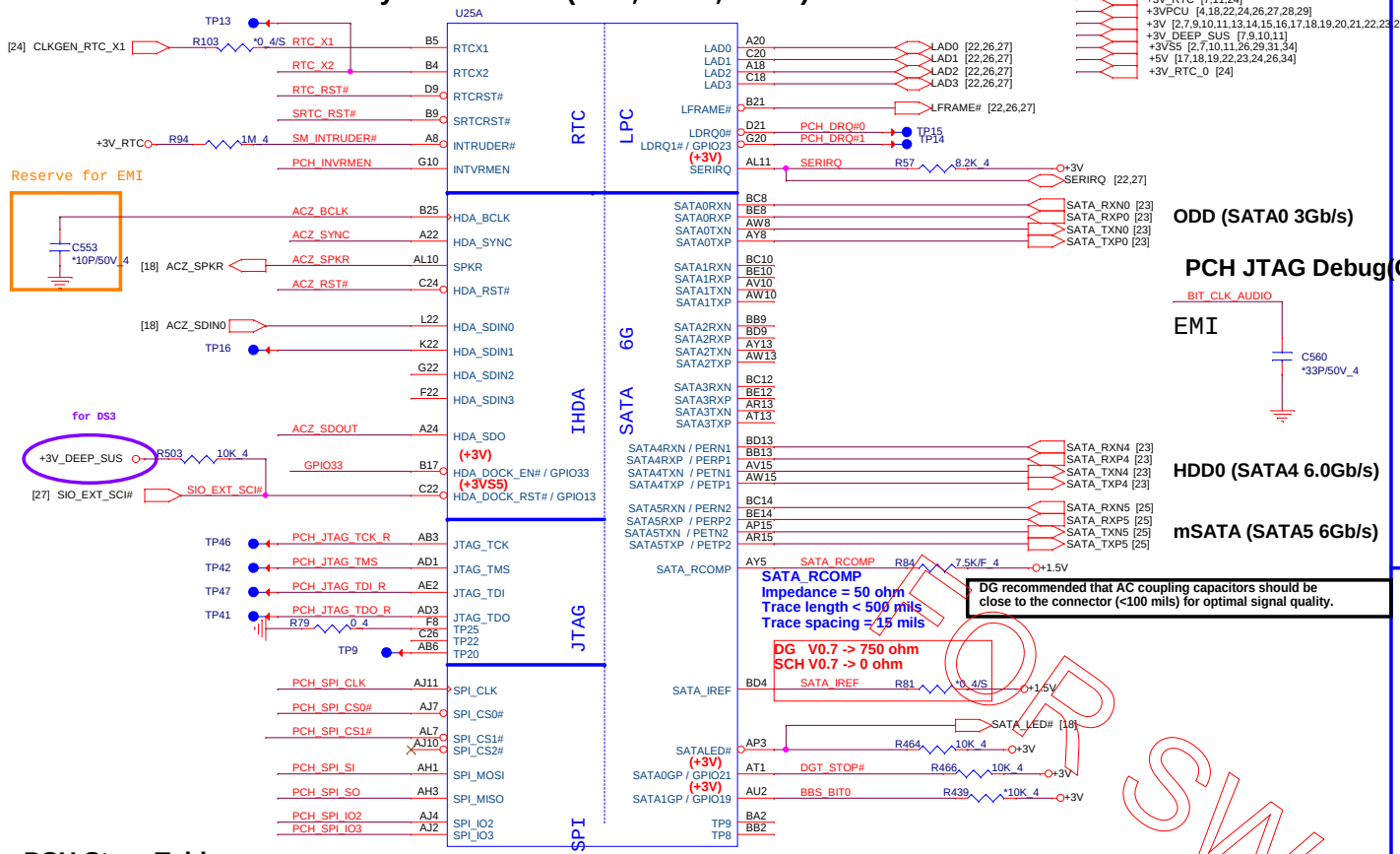
Lynx Point (HDA,JTAG,SATA)

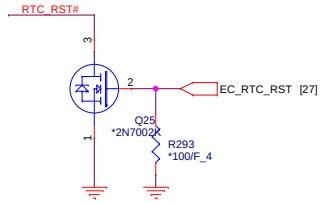


PCH Strap Table

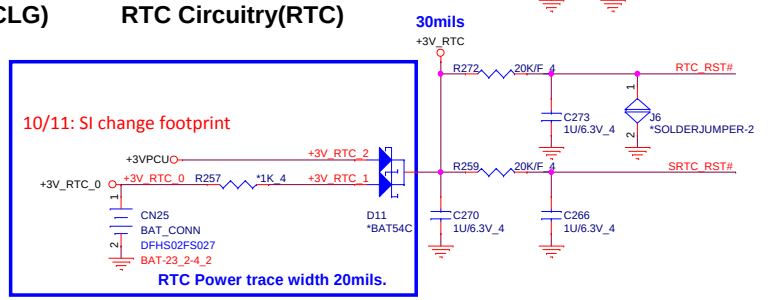
Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R58 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (Int PU)	R32 *1K_4 PCI_GNT3# [9]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	0 = Disable 1 = Enable	PCH_INVRMEN R96 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R488 *0_4 +3V [Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# 1, GNT0# 1: SPI; GNT1# 0, GNT0# 0: LPC	BBS_BIT0 R467 *1K_4 R105 *1K_4 BBS_BIT1 [9]
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+VCC_HDA_IO R499 *1K_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Security Effect (Int PD) 1 = Can be Overridden	[27] GPIO33_EC ACZ_SDOUT R504 *1K_4 +VCC_HDA_IO
SATA2GP/GPIO36	DMI RX Termination	PLTRST#	0 = DMI RX is terminated to VSS 1 = DMI RX is terminated to VCC/2	[10] DGPU_PWR_EN_R DGPU_PWR_EN_R R465 *1K_4 +3V
SATA3GP/GPIO37	TLS Confidentiality	PLTRST#	0 = TLS no confidentiality (Int PD) 1 = TLS with confidentiality	[10] FDI_OVRVLTG FDI_OVRVLTG R432 *1K_4 +3V
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	R30 *1K_4 PCH_SUSCLK [7]

08

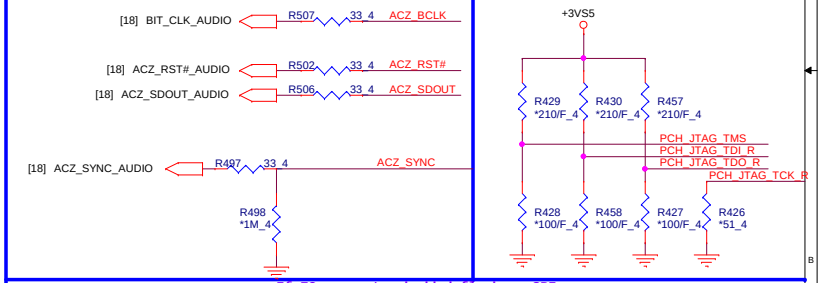
RTC Clock 32.768KHz



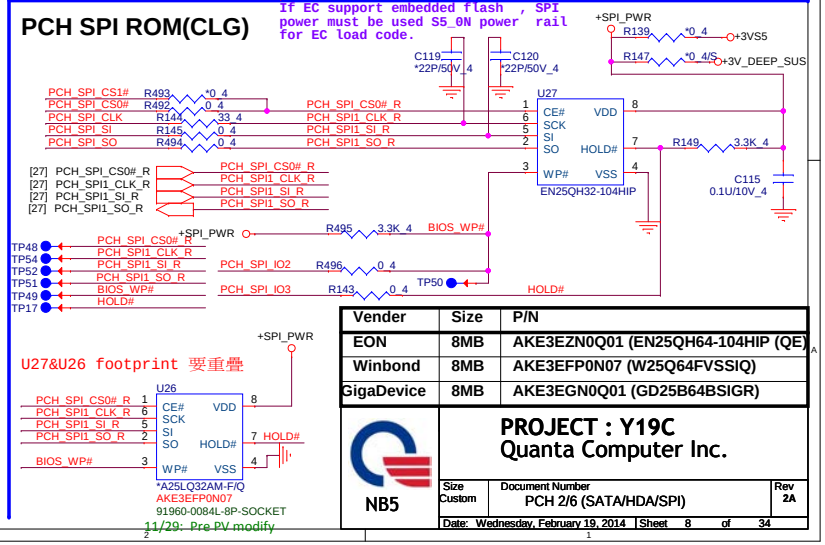
RTC Circuitry(RTC)



HDA Bus(CLG)



PCH SPI ROM(CLG)



Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP (QE)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)

NB5

PROJECT : Y19C
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	2A

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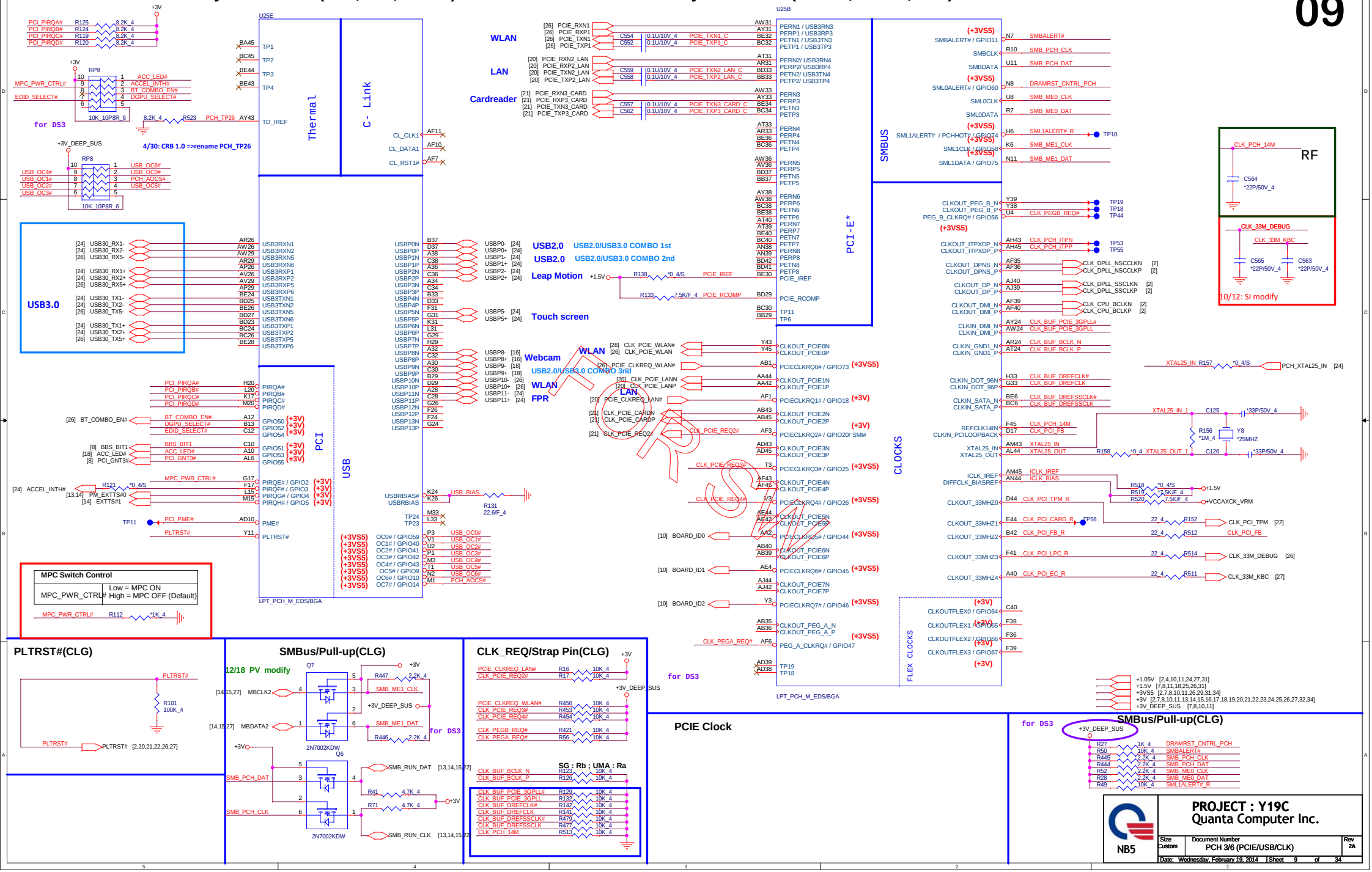
Lynx Point (PCI,USB,NVRAM)

Lynx Point (PCI-E,SMBUS,CLK)

09



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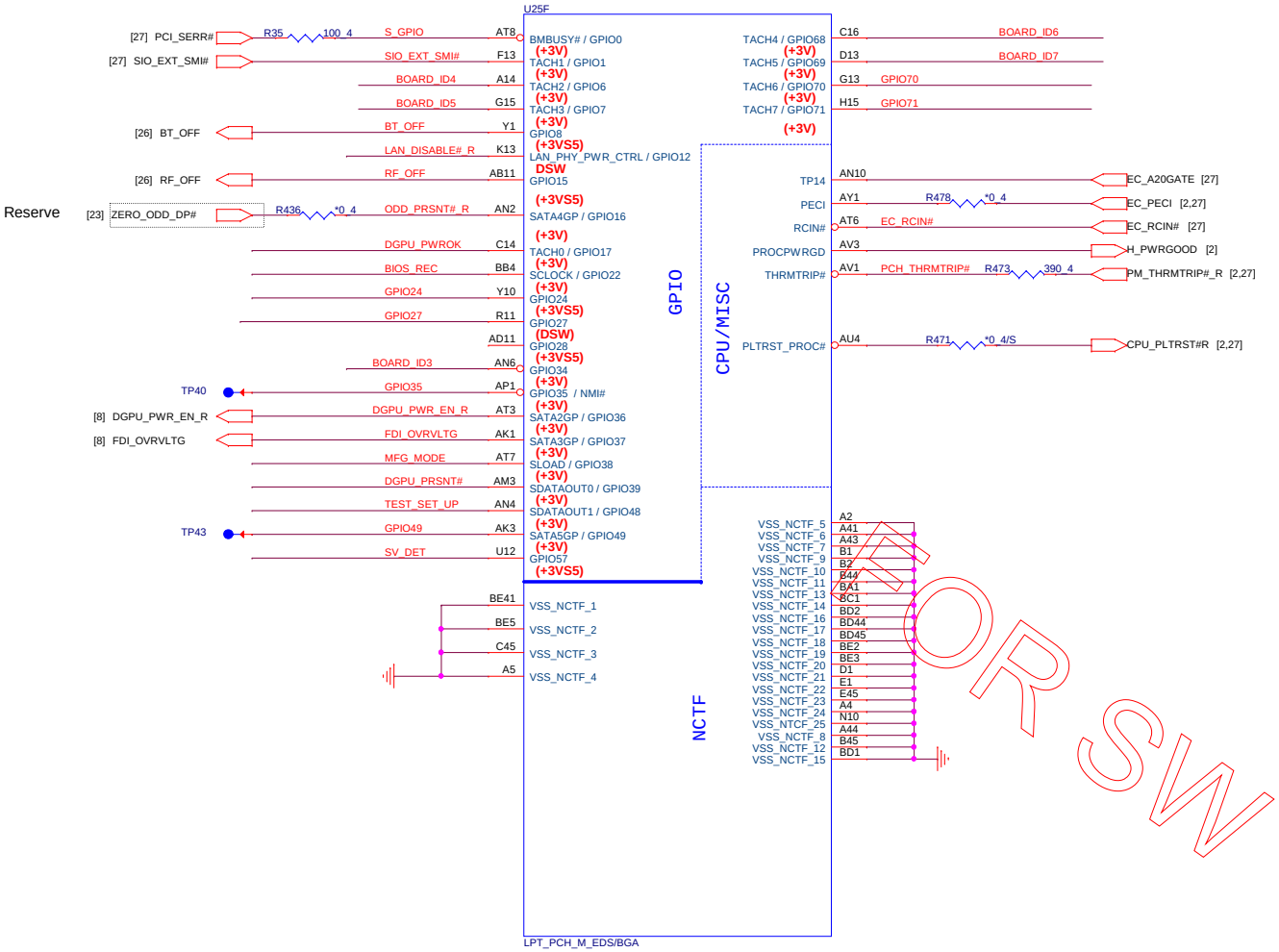
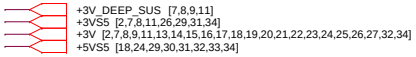
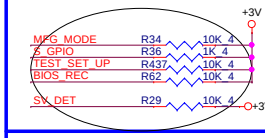
Lynx Point (GPIO,VSS_NCTF,RSVD)



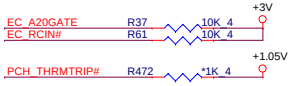
OR SW

Clock Gen Power OK (CLG)

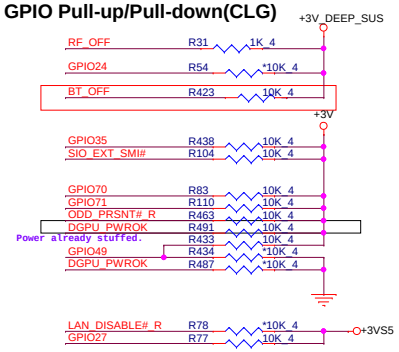




PCH MISC PU /PD

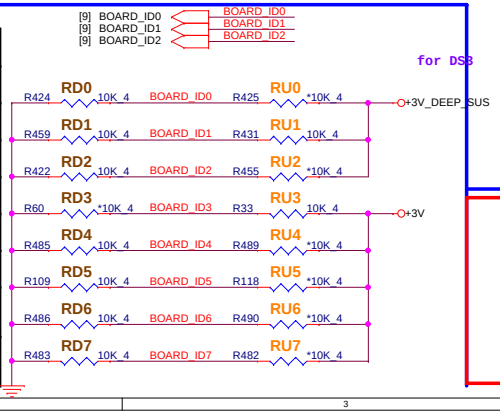


GPIO Pull-up/Pull-down(CLG)



BOARD ID SETTING

Model	BOARD_ID7	BOARD_ID5	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
Pavillian 14"	0	0	0	0	0	0	0	0
Pavillian 15.6"	0	0	0	0	0	0	1	0
Pavillian 17"	0	0	0	0	0	1	0	0
Envy 14"	0	0	0	0	1	0	0	0
Envy 15.6"	0	0	0	0	1	0	1	0
Envy 17"	0	0	0	0	1	1	0	0



GFX Present

	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

NB5

PROJECT : Y19C
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	2A

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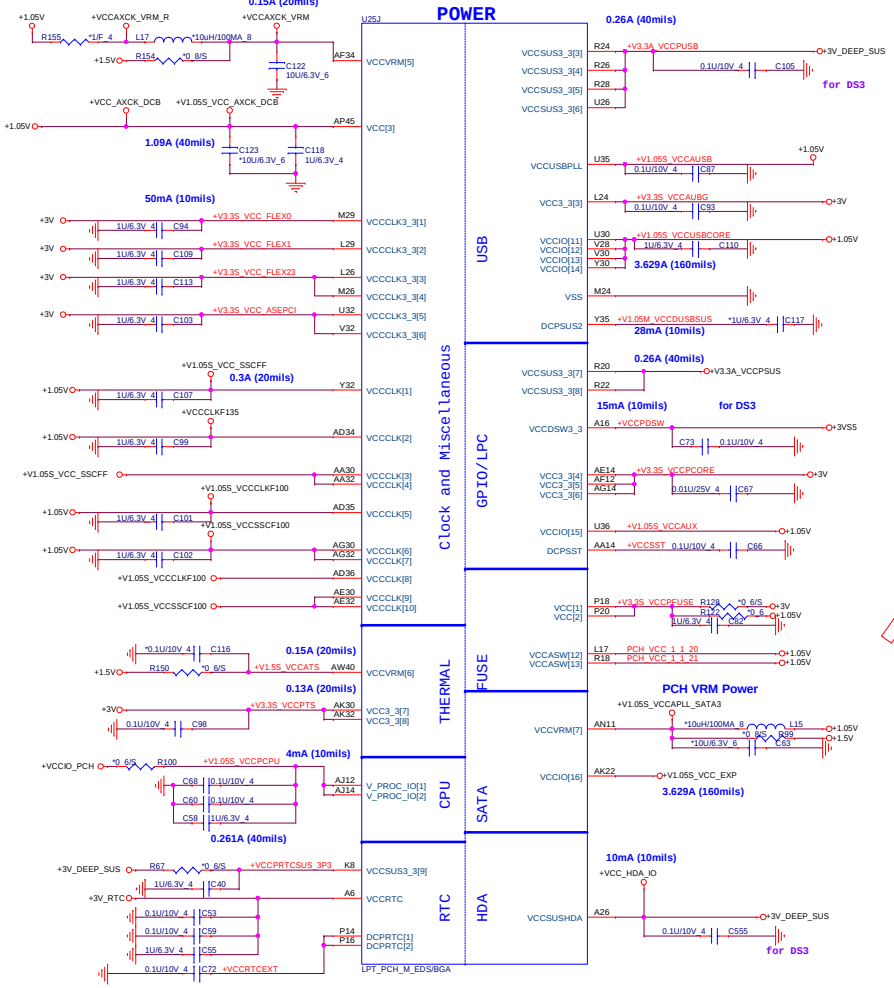
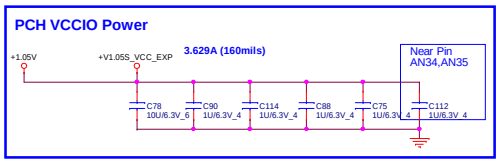
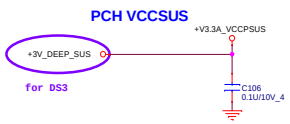
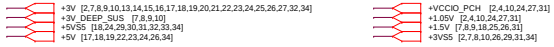
Lynx Point (POWER)

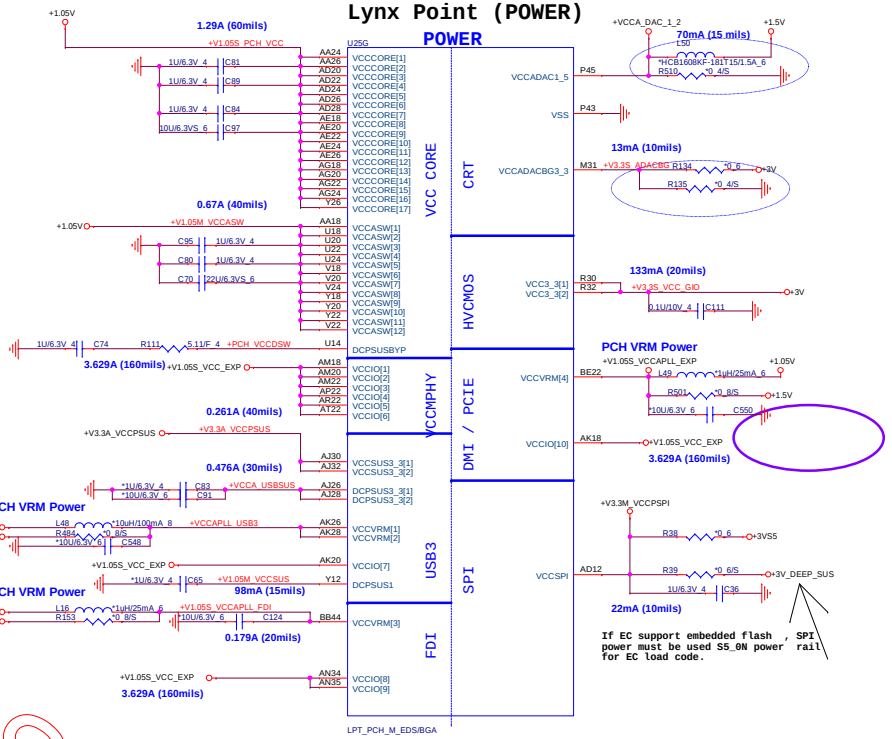


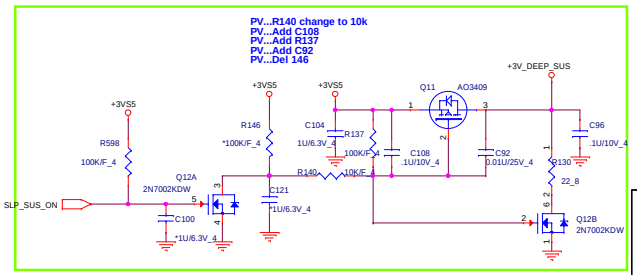






Lynx Point (POWER)





NB5

PROJECT : Y19C
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 5/6 (POWER)	2A

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FOR SW

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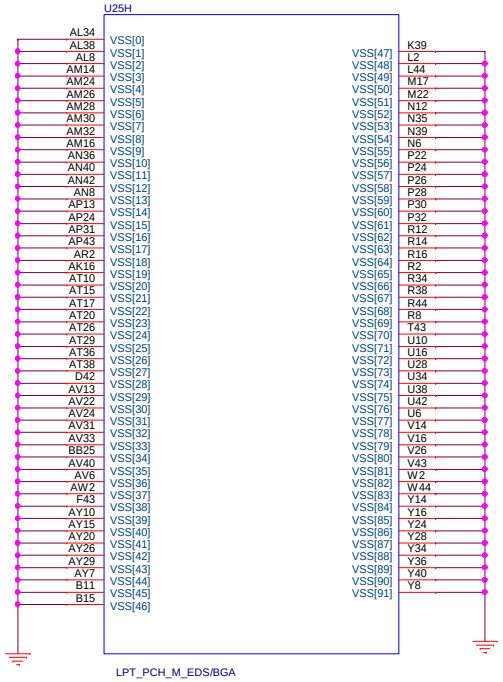
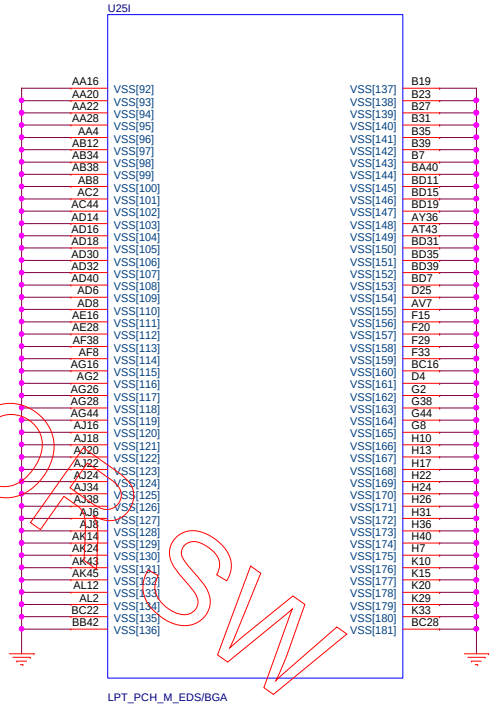
Lynx Point (GND)



Lynx Point (GND)



FOR SW

[20,24,34] +3VLANVCC
[8,24] +3V_RTC_0
[4,8,18,22,24,26,27,28,29] +3VPCU
[2,4,10,11,24,27,31] +1.05V

NB5

PROJECT : Y19C
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 6/6 (GND)	2A

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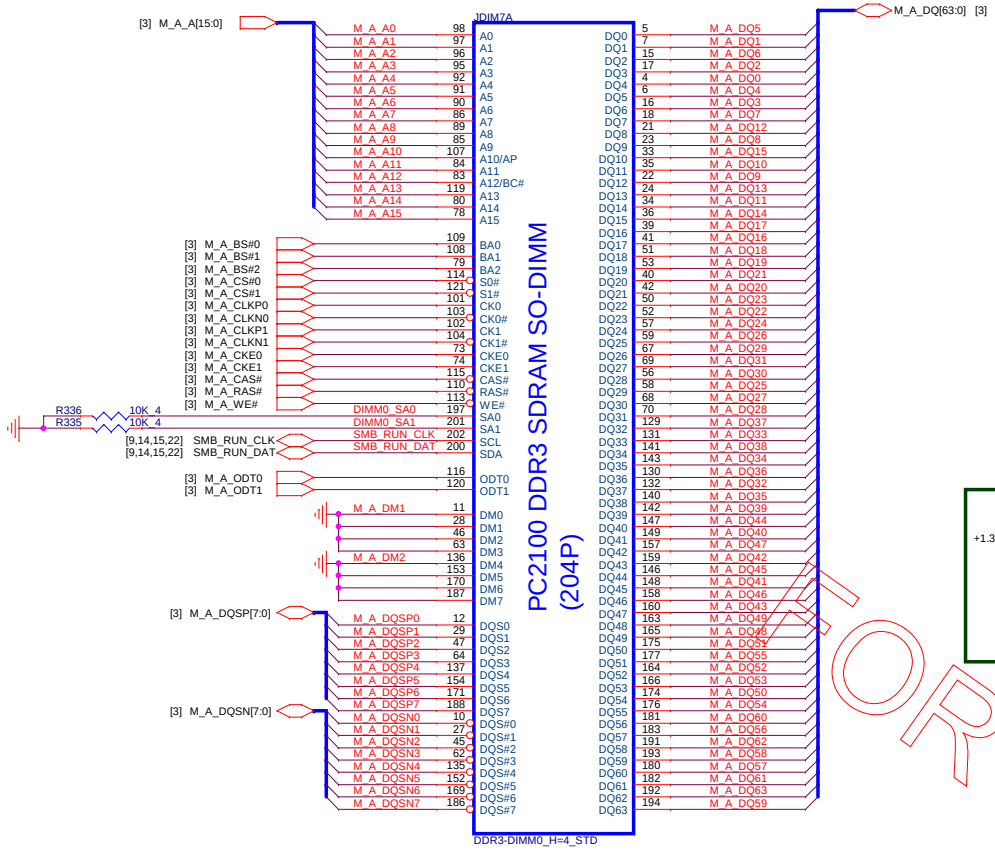
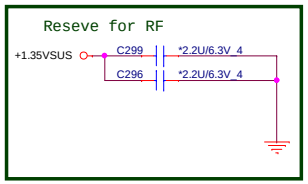
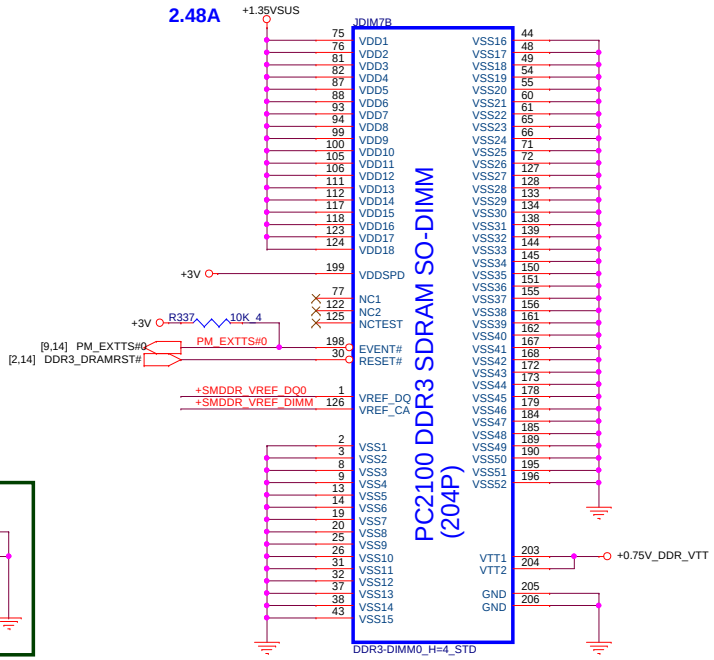
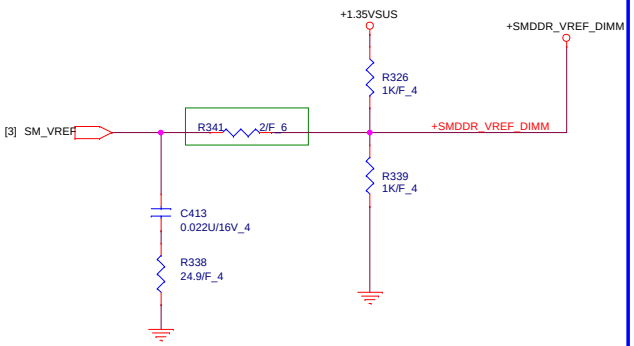




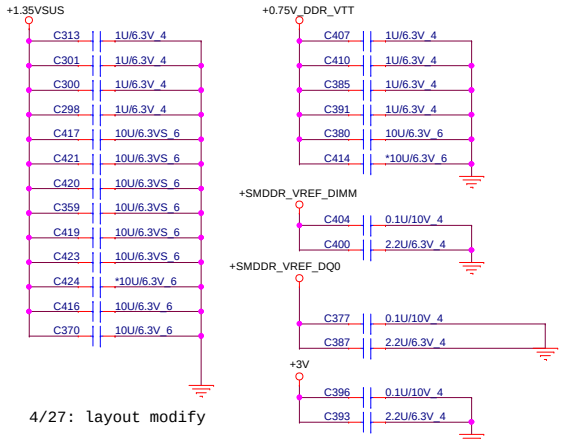


+SMDDR_VREF_DIMM [14]
+0.75V_DDR_VTT [14,30,34]
+1.35VSUS [2,4,14,17,30]
+3V [2,7,8,9,10,11,14,15,16,17,18,19,20,21,22,23,24,25,26,27,32,34]

FOR SW

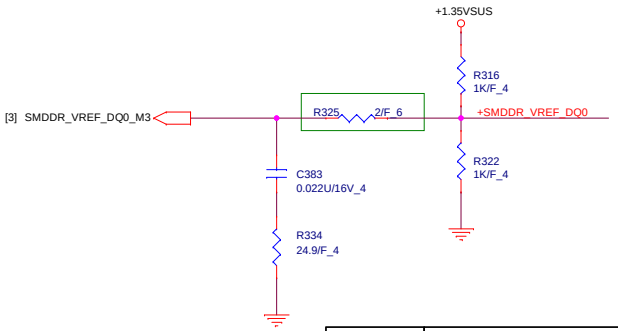


Place these Caps near So-Dimm0.



4/27: layout modify

VREF DQ0 M1 Solution



NB5

PROJECT : Y19C
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM0-RVS (5.2H)	2A

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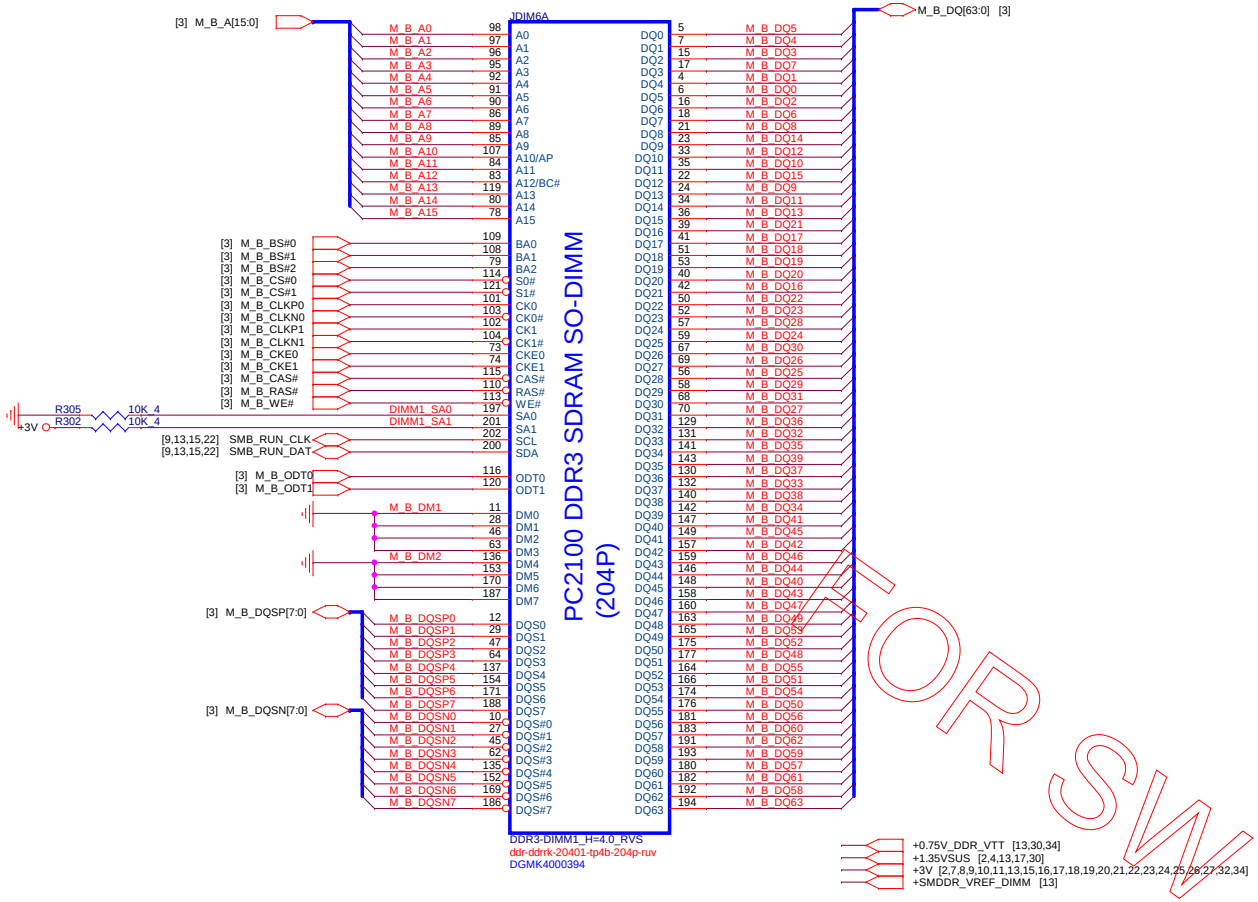
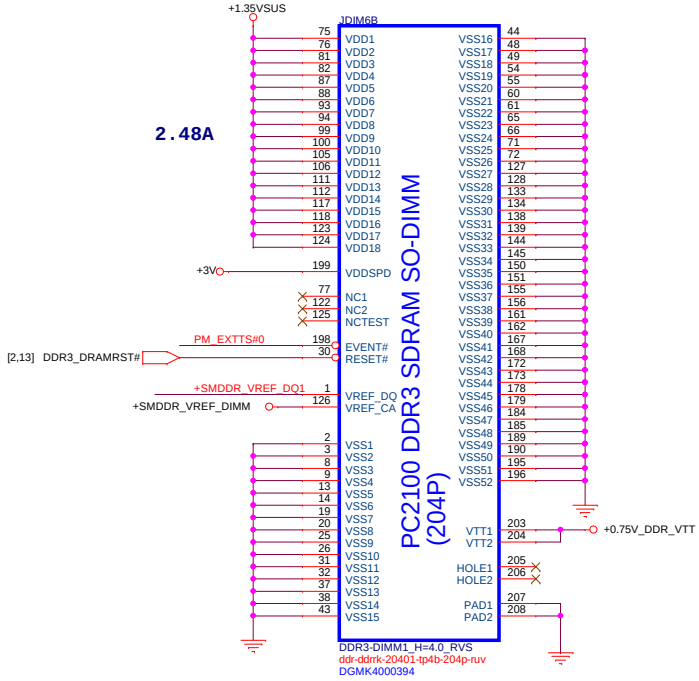
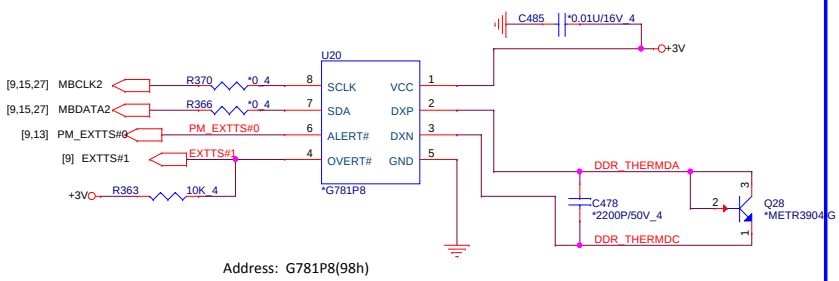




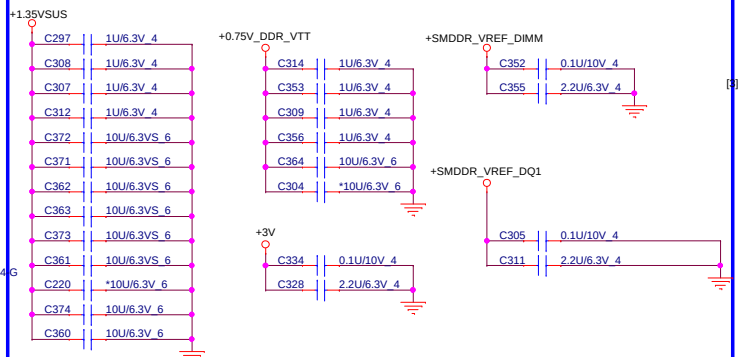
FOR SW

DDR Thermal Sensor

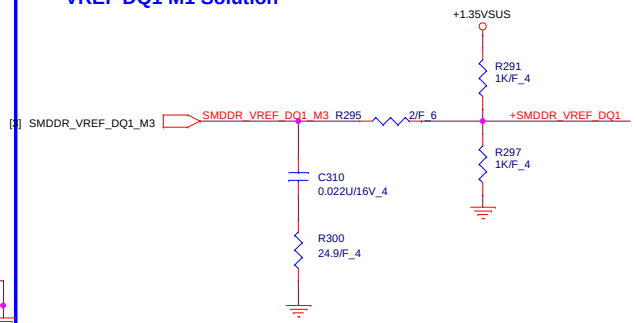


Address: G781P8(98h)

Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution



NB5

PROJECT : Y19C
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM1-RVS (9.2H)	2A

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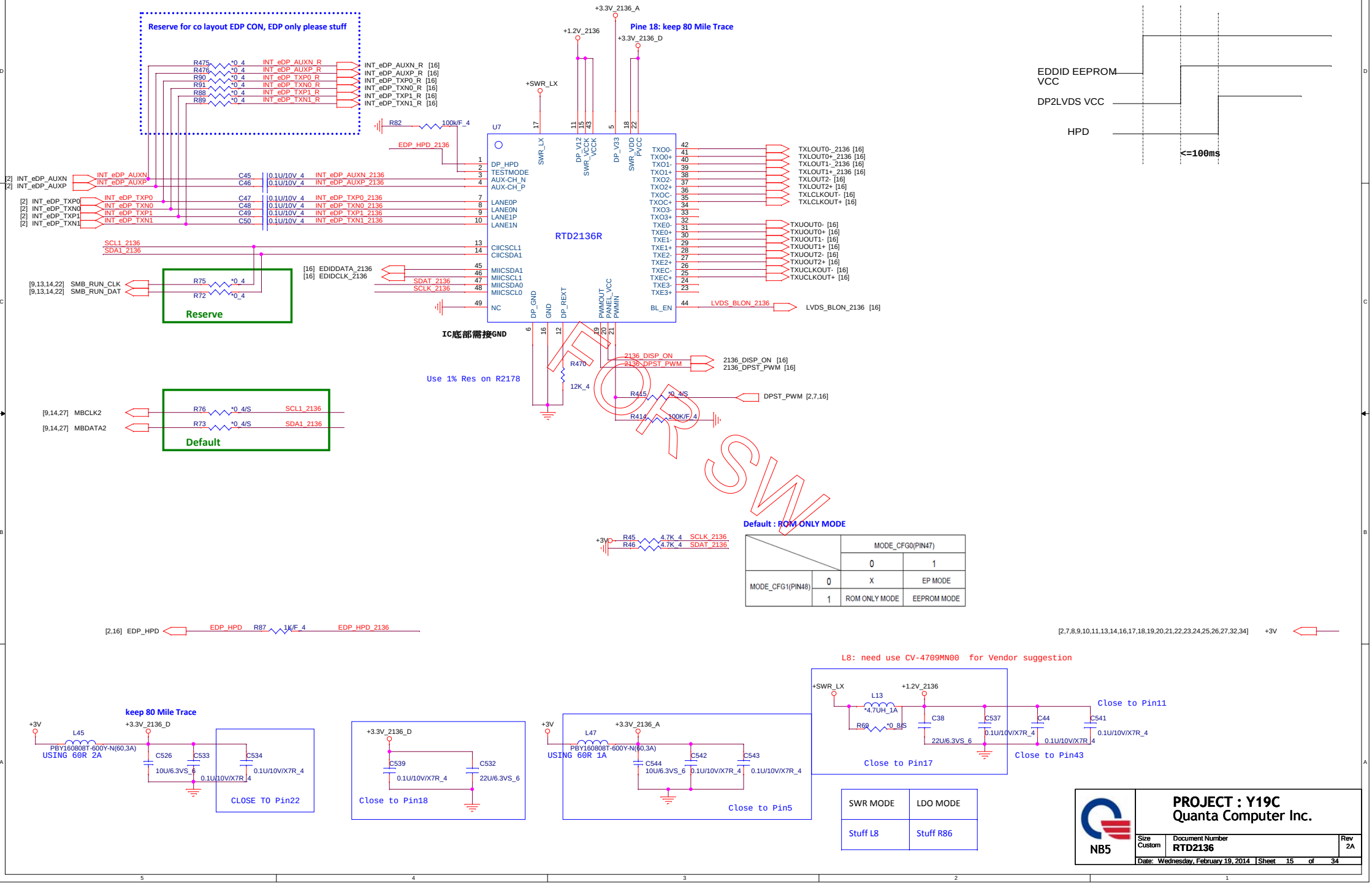
RTD2136 Dual Channel only



	MODE_CFG0(PIN47)	
	0	1
MODE_CFG1(PIN48) 0	X	EP MODE
MODE_CFG1(PIN48) 1	ROM ONLY MODE	EEPROM MODE

SWR MODE	LDO MODE
Stuff L8	Stuff R86

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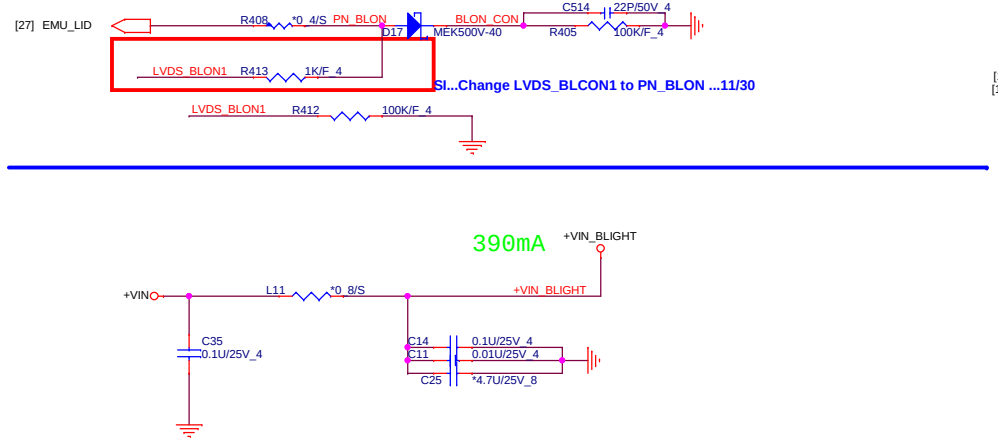
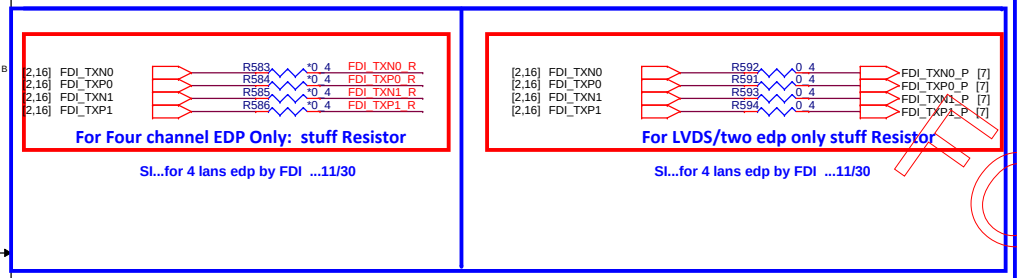
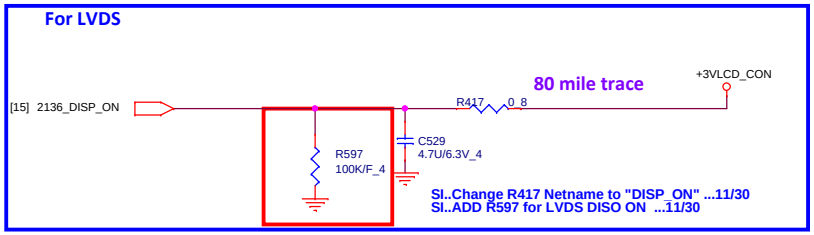
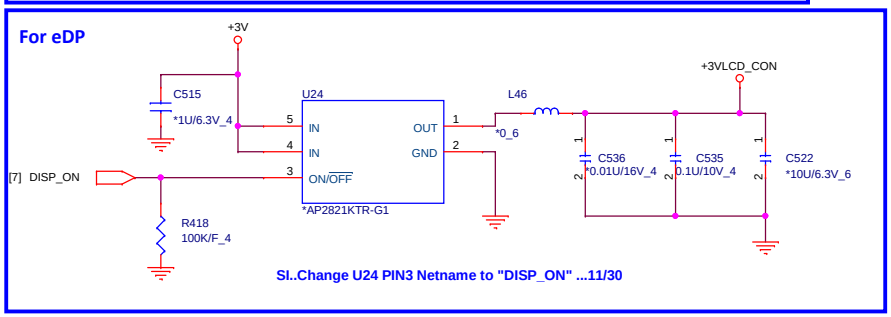
LID

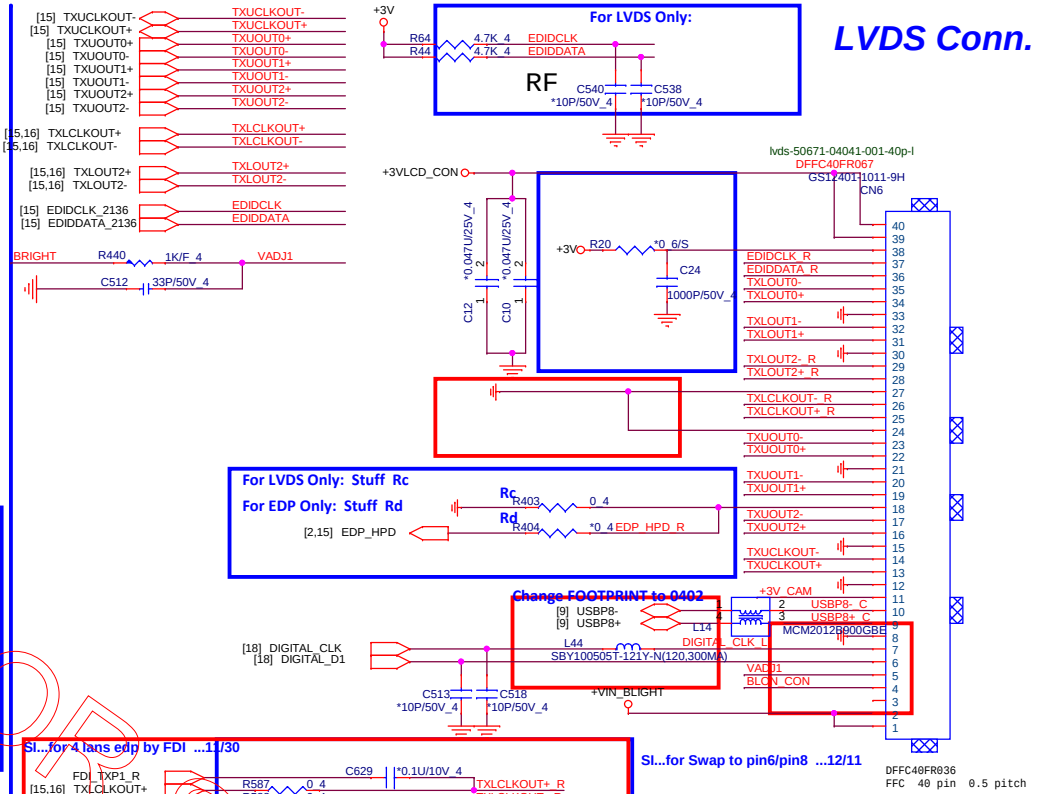


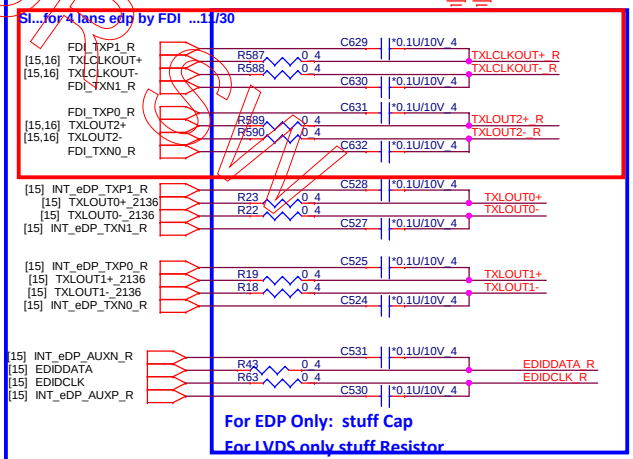


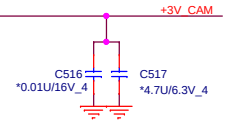


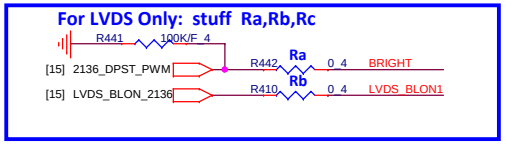


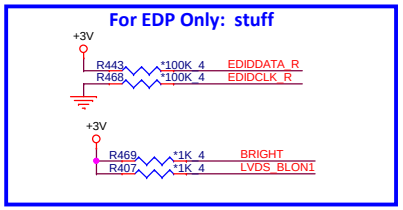
[2,7,8,9,10,11,13,14,15,17,18,19,20,21,22,23,24,25,26,27,32,34] +3V
[4,8,18,22,24,26,27,28,29] +3VPCU
[17,18,19,22,23,24,26,34] +5V
[19,22,23,28,29,30,31,32,34] +VIN

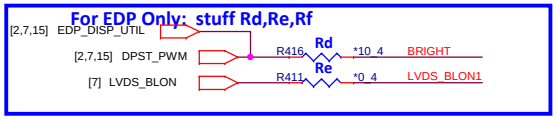












LVDS Conn.

16

NB5

PROJECT : Y19C
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	2A

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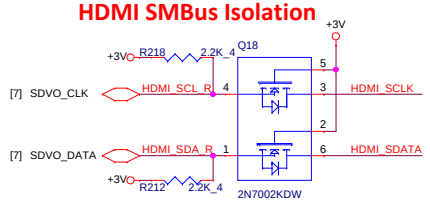
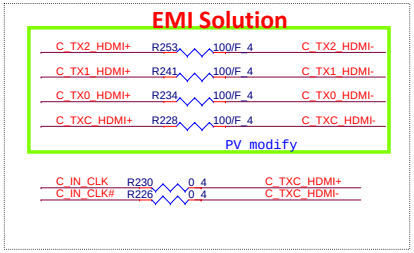
HDMI Conn.

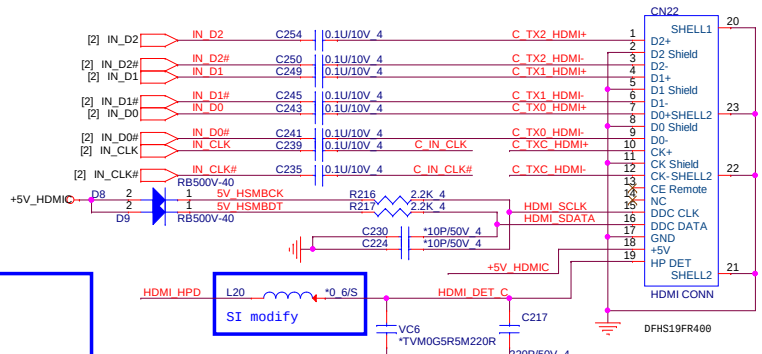
HDMI SMBus Isolation

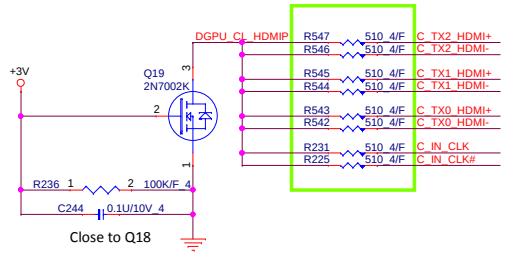


Close to HDMI connector

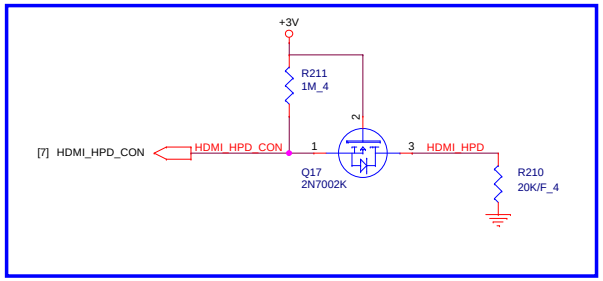
EMI Solution

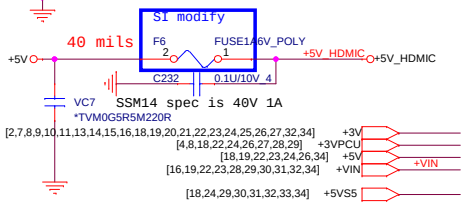


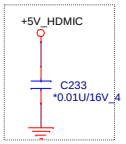




Close to Q18



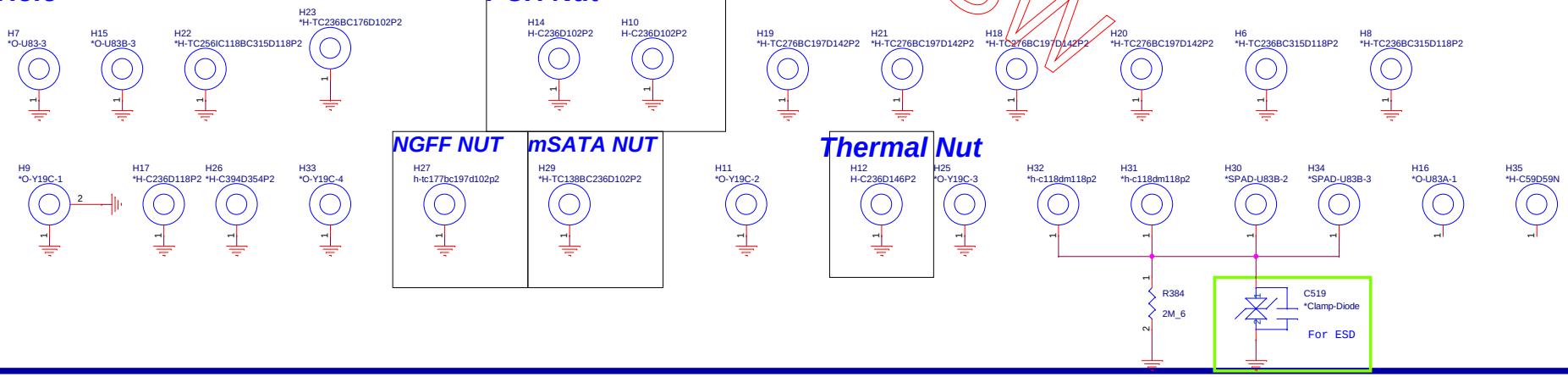




for EMI request

FOR SW

Hole



PCH Nut

H14 H-C236D102P2
H10 H-C236D102P2

NGFF NUT

H27 h-tc177bc197d102p2

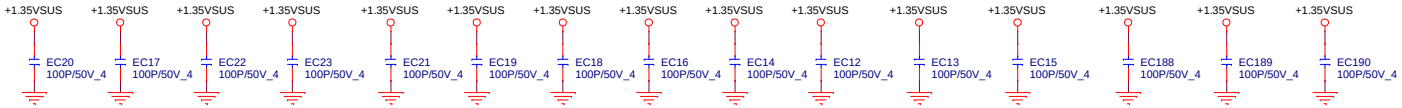
mSATA NUT

H29 *H-TC138BC236D102P2

Thermal Nut

H12 H-C236D146P2
H25 *O-Y19C-3

EMI



NB5

PROJECT : Y19C
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI	2A

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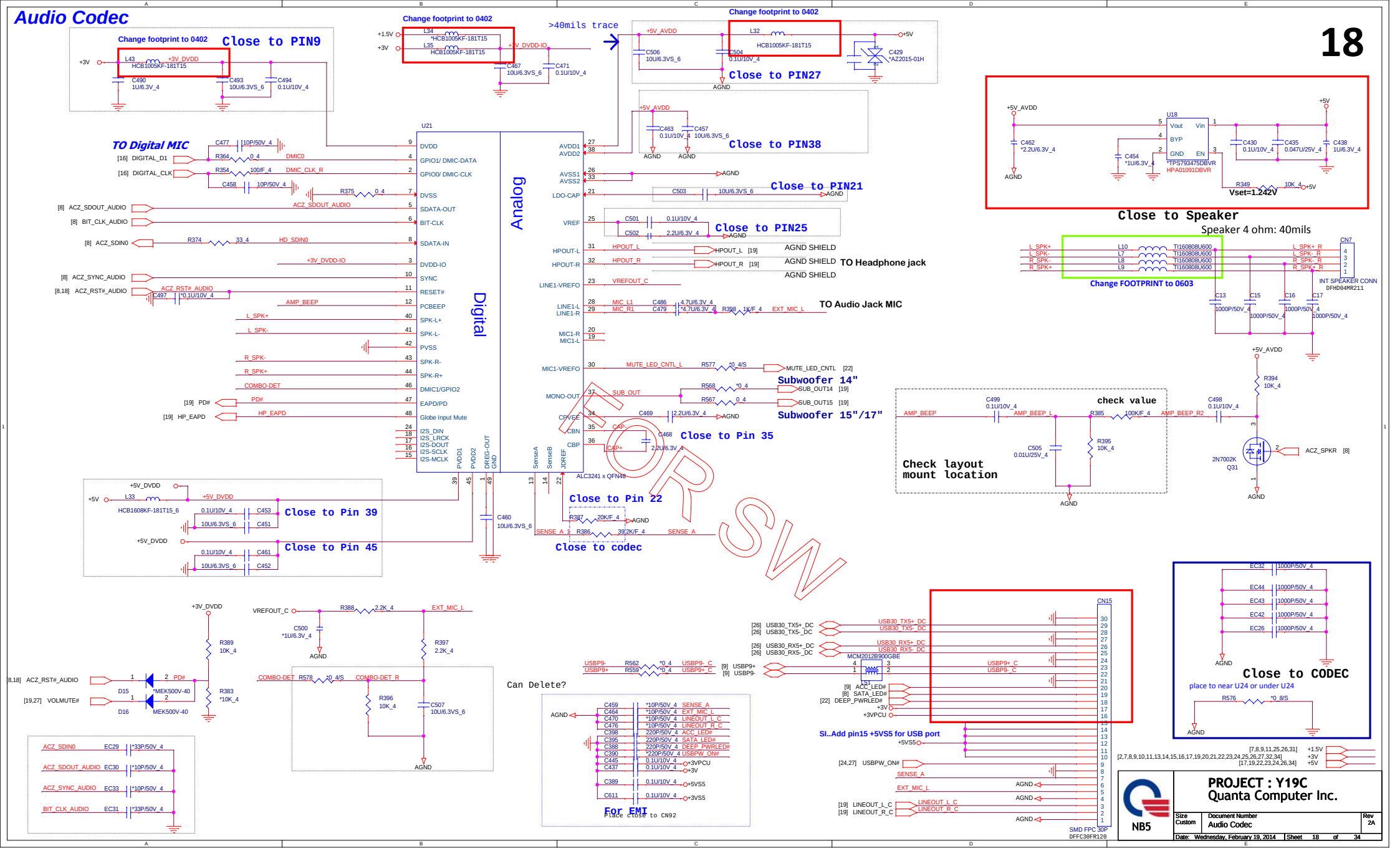
Audio Codec



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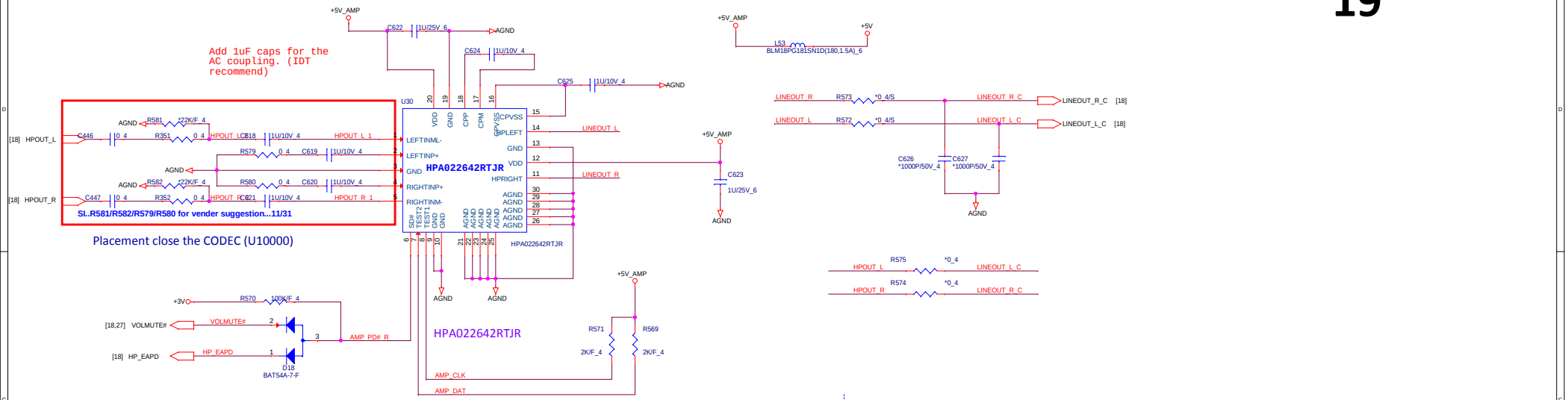
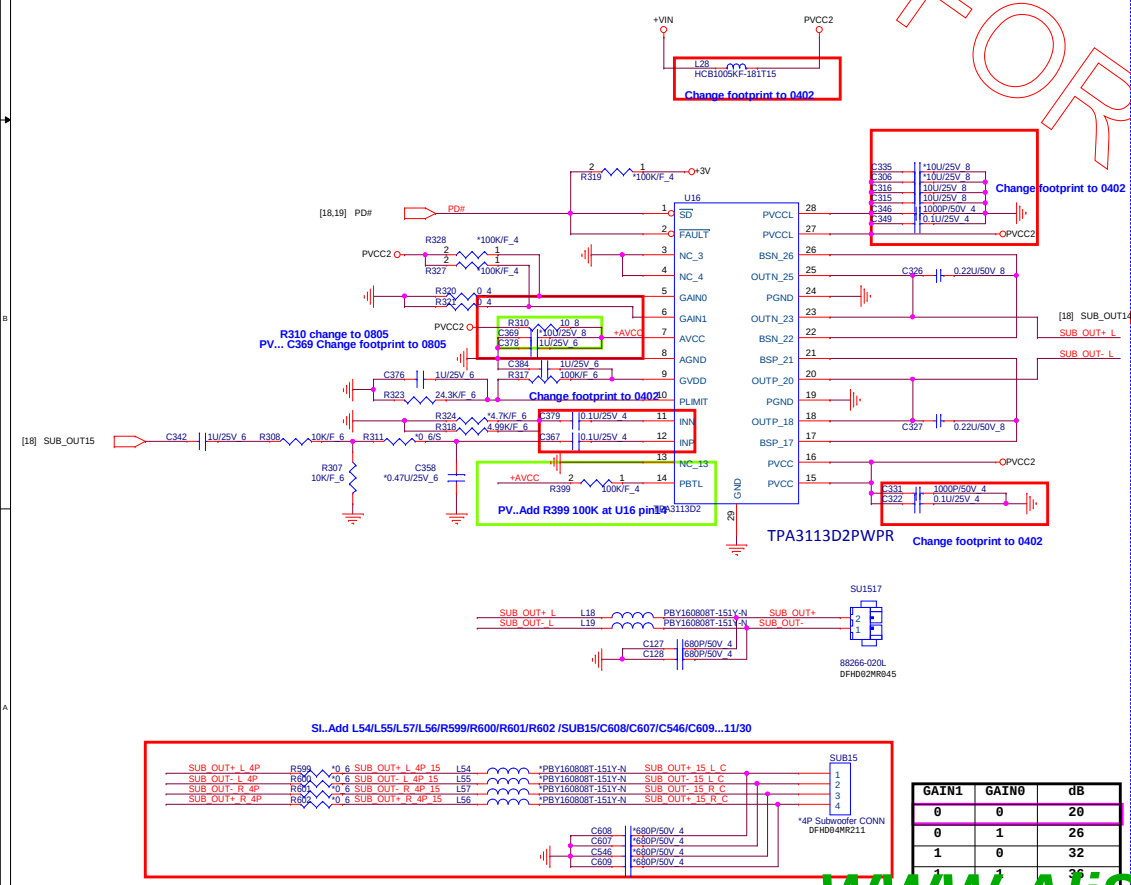
Head Phone out

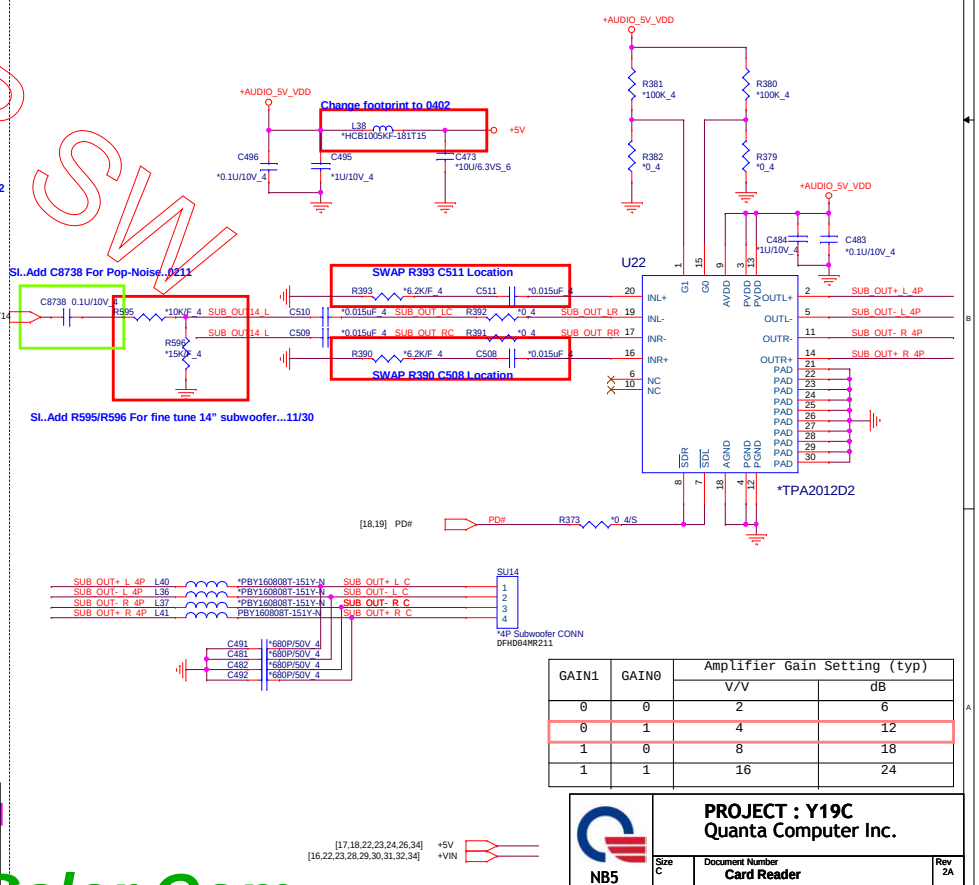


Subwoofer 15"/17"



GAIN1	GAIN0	dB
0	0	20
0	1	26
1	0	32
1	1	36

Subwoofer 14"



GAIN1	GAIN0	Amplifier Gain Setting (typ)	
		V/V	dB
0	0	2	6
0	1	4	12
1	0	8	18
1	1	16	24

[17,18,22,23,24,26,34] +5V
[16,22,23,28,29,30,31,32,34] +VIN

PROJECT : Y19C
Quanta Computer Inc.

NB5

Size	Document Number	Rev
C	Card Reader	2A

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FOR SW
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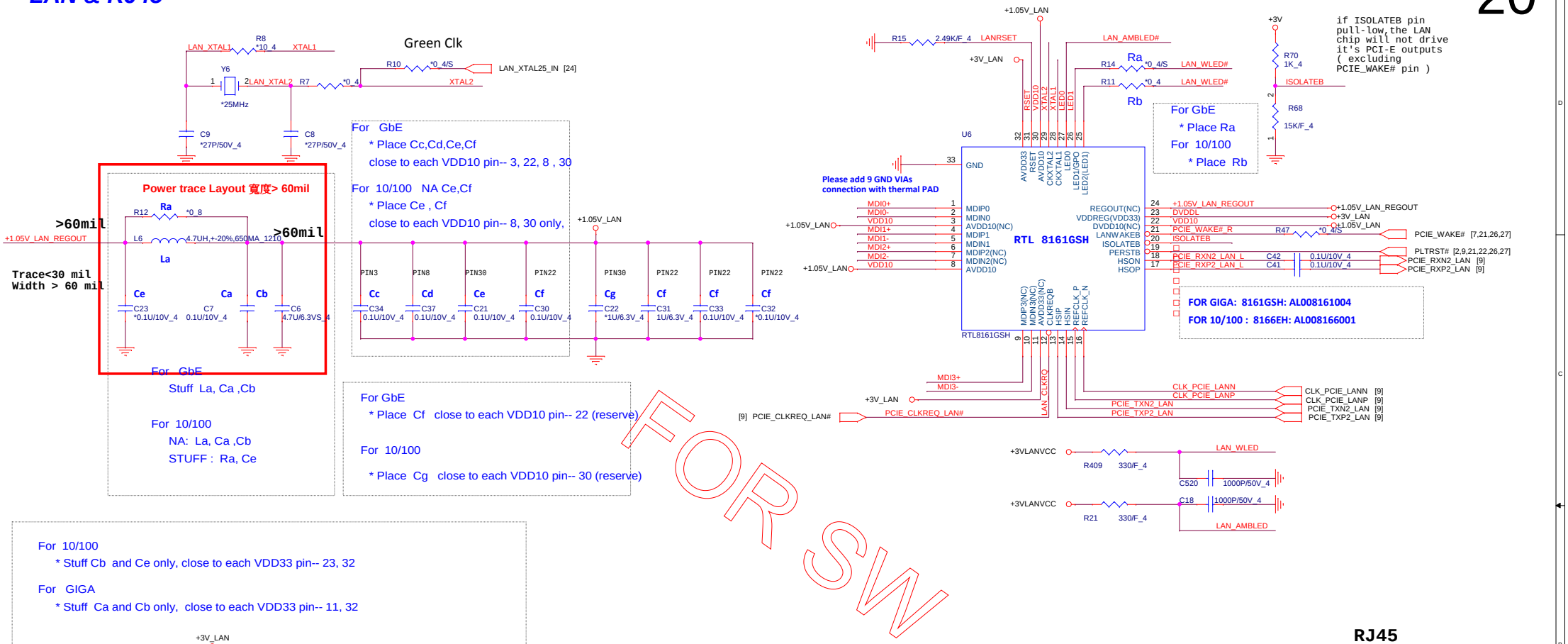
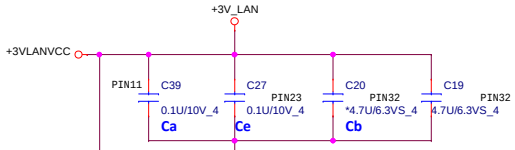
LAN & RJ45

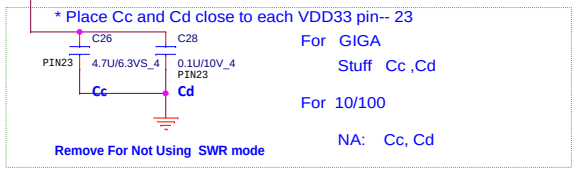


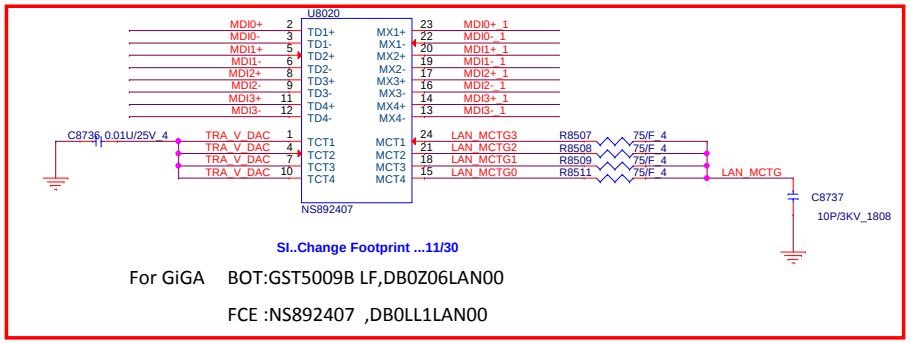
FOR SW

For 10/100
* Stuff Cb and Ce only, close to each VDD33 pin-- 23, 32

For GIGA
* Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32







SI..Change Footprint ...11/30

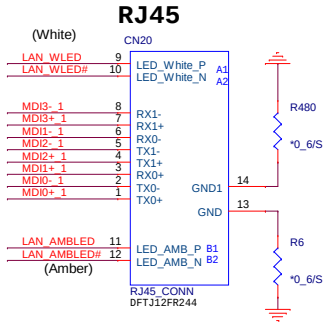
For GiGA BOT:GST5009B LF,DB0Z06LAN00

FCE :NS892407 ,DB0LL1LAN00

For 10/100

BOT: TST1284R LF DB0EL5LAN00

FCE :NS892408 ,DB0EF7LAN01



[2,7,8,9,10,11,13,14,15,16,17,18,19,21,22,23,24,25,26,27,32,34] +3V
[24,34] +3VLANVCC

NB5	PROJECT : Y19C Quanta Computer Inc.	
Size Custom	Document Number RTL 8161/RJ45	Rev 2A
Date: Wednesday, February 19, 2014	Sheet 20 of 34	

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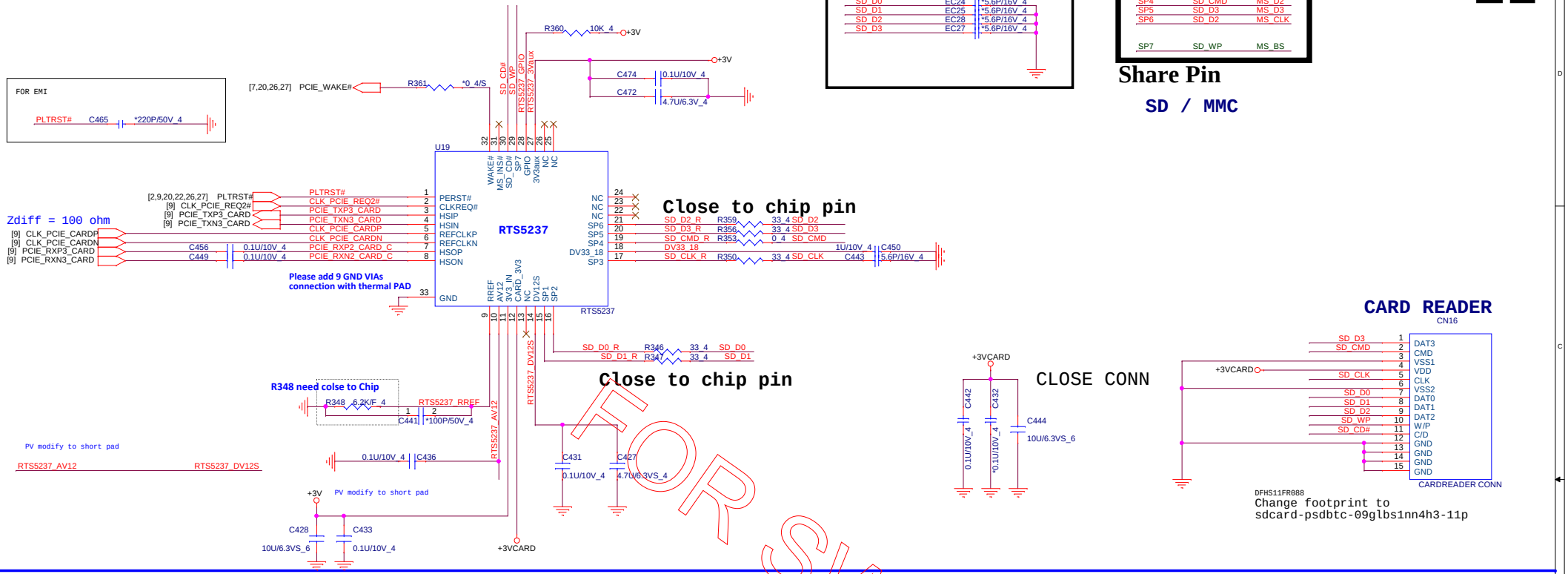
CardReader



FOR SW

NB5

PROJECT : Y19C
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CR RTS5237 & CR SOCKET	2A

Date: Wednesday, February 19, 2014 | Sheet 21 of 34

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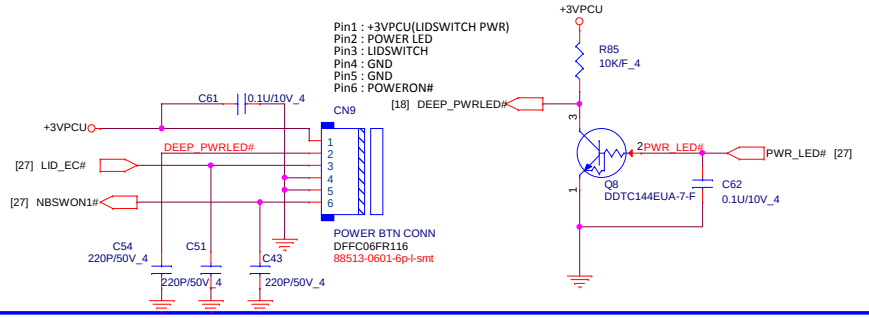
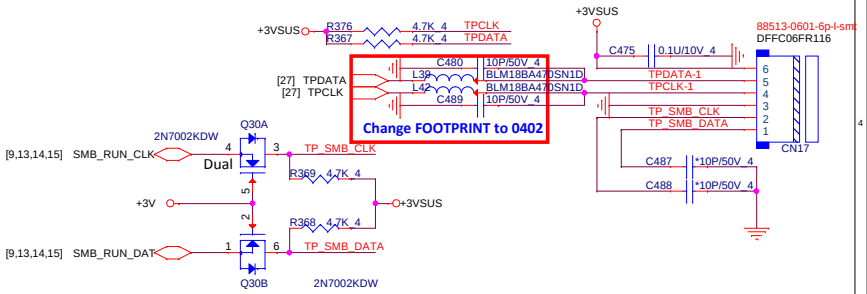
Power Botton Connector

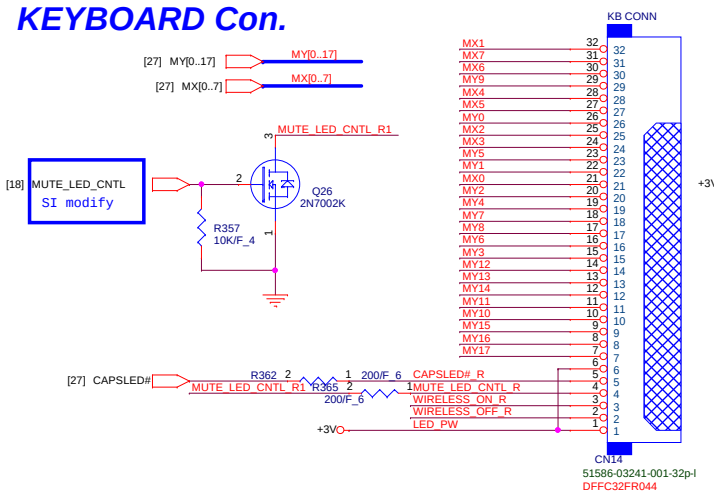


Touch Pad Connector

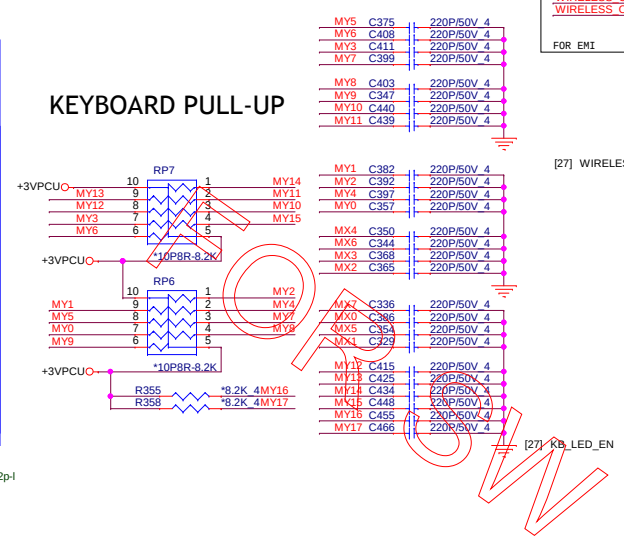
25 mils

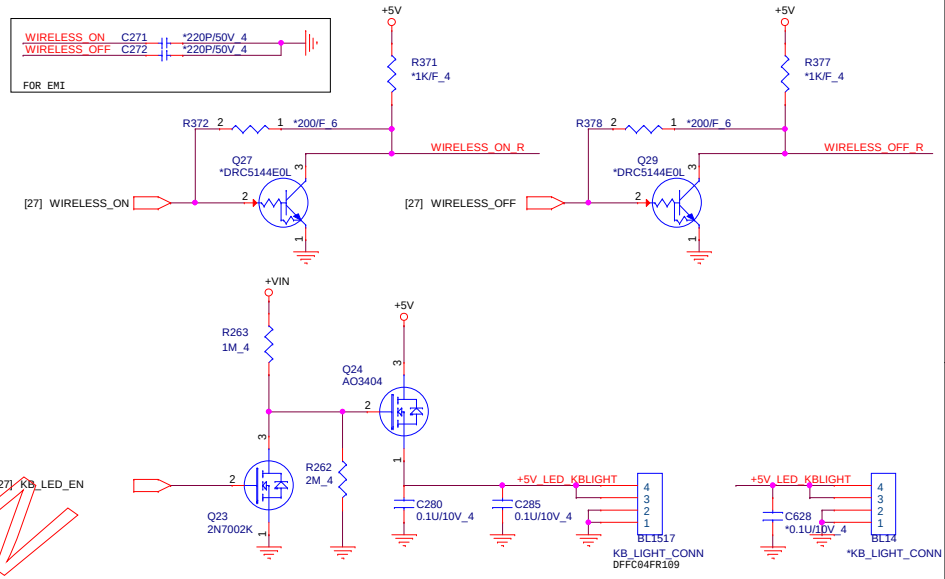


KEYBOARD Con.



KEYBOARD PULL-UP

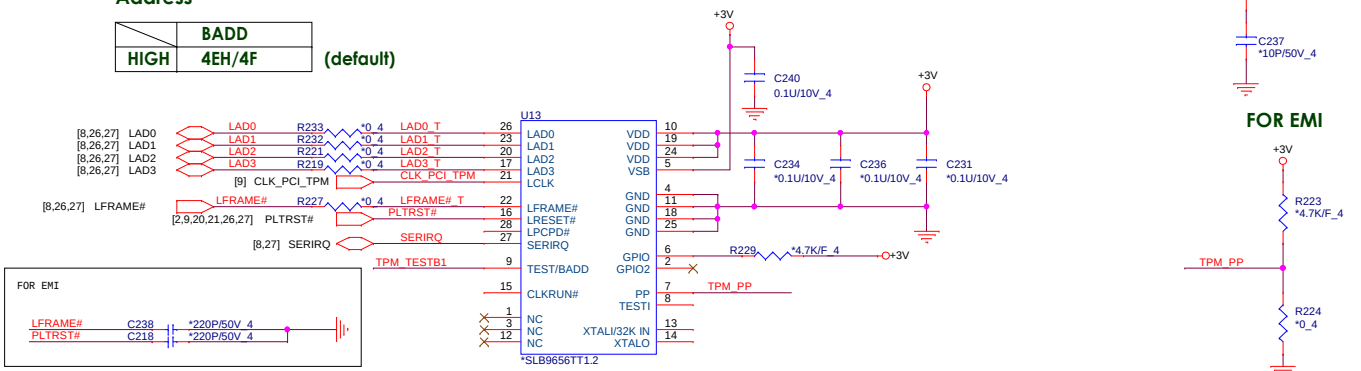




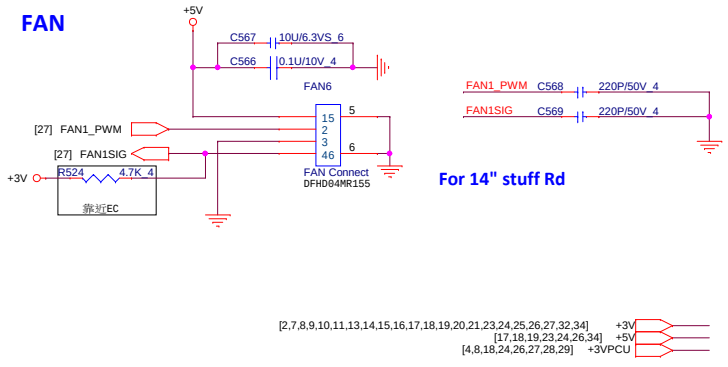
TPM (1.2)

Address

	BADD
HIGH	4EH/4F (default)



FAN



NB5

PROJECT : Y19C
Quanta Computer Inc.

Size	Document Number	Rev
Custom	TPM/TP/FAN/LED	2A

Date: Wednesday, February 19, 2014 | Sheet 22 of 34

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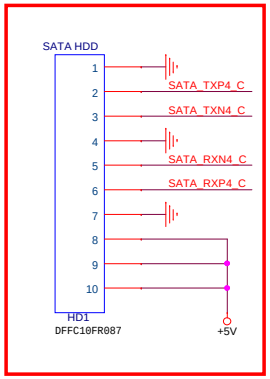
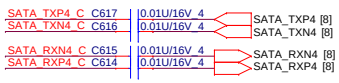
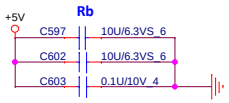
SATA HDD Connector(Cable type)

+5V: 2 A(4 Pin)
Gnd : (5 Pin)
+3V: 2 A(4 Pin)



SI...HD1 Pin-define...11/25

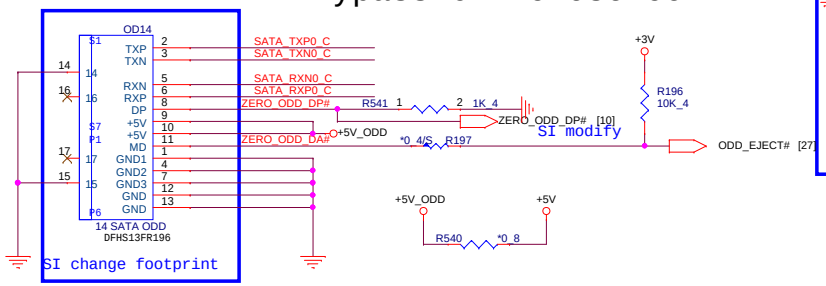


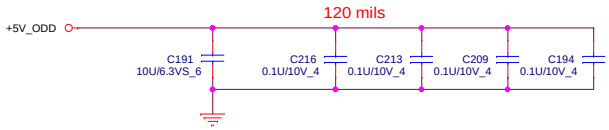


SATA ODD CONNECTOR

14" SATA ODD

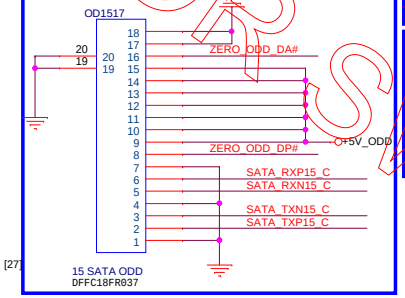
Bypass CAP close conn

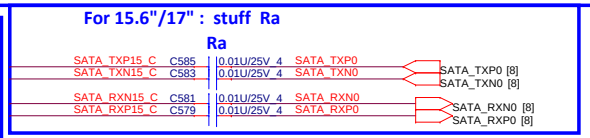


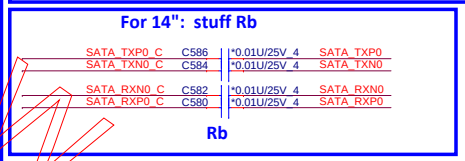


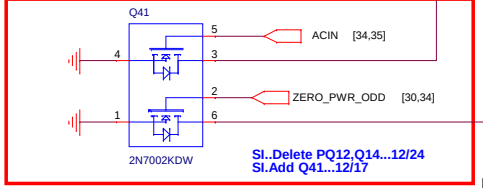
15"/17" SATA ODD

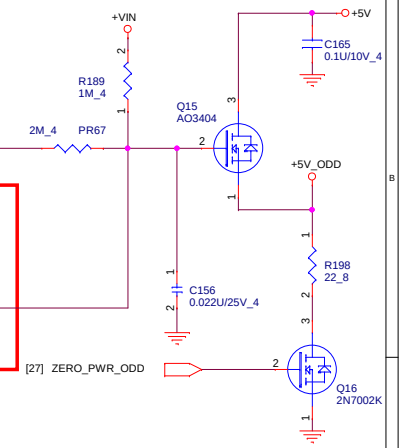
New Type











High : ODD power down
Low : ODD power on

[2,7,8,10,11,26,29,31,34] +3VS5

NB5

PROJECT : Y19C
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDD/ODD	2A

Date: Wednesday, February 19, 2014 | Sheet 23 of 34

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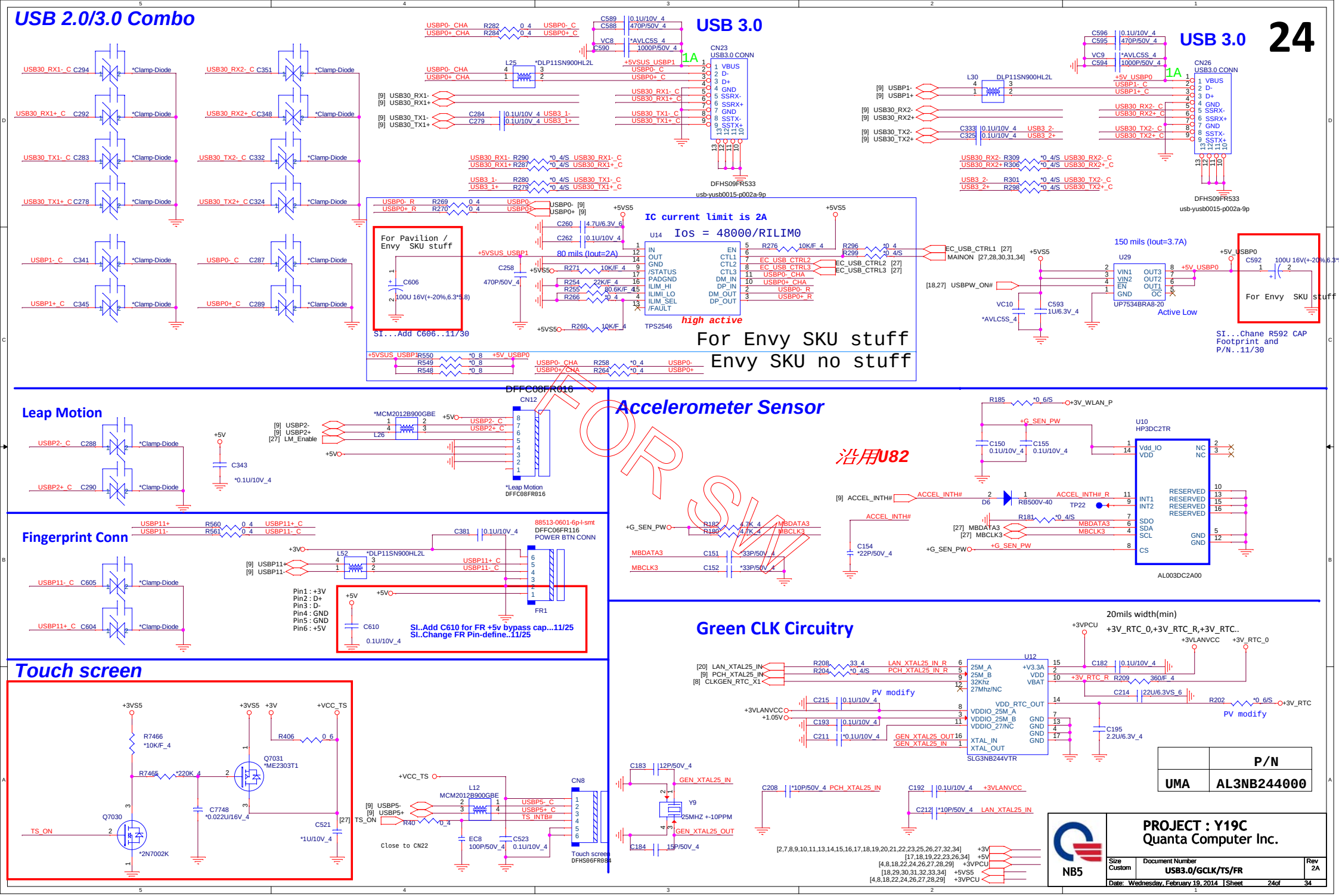

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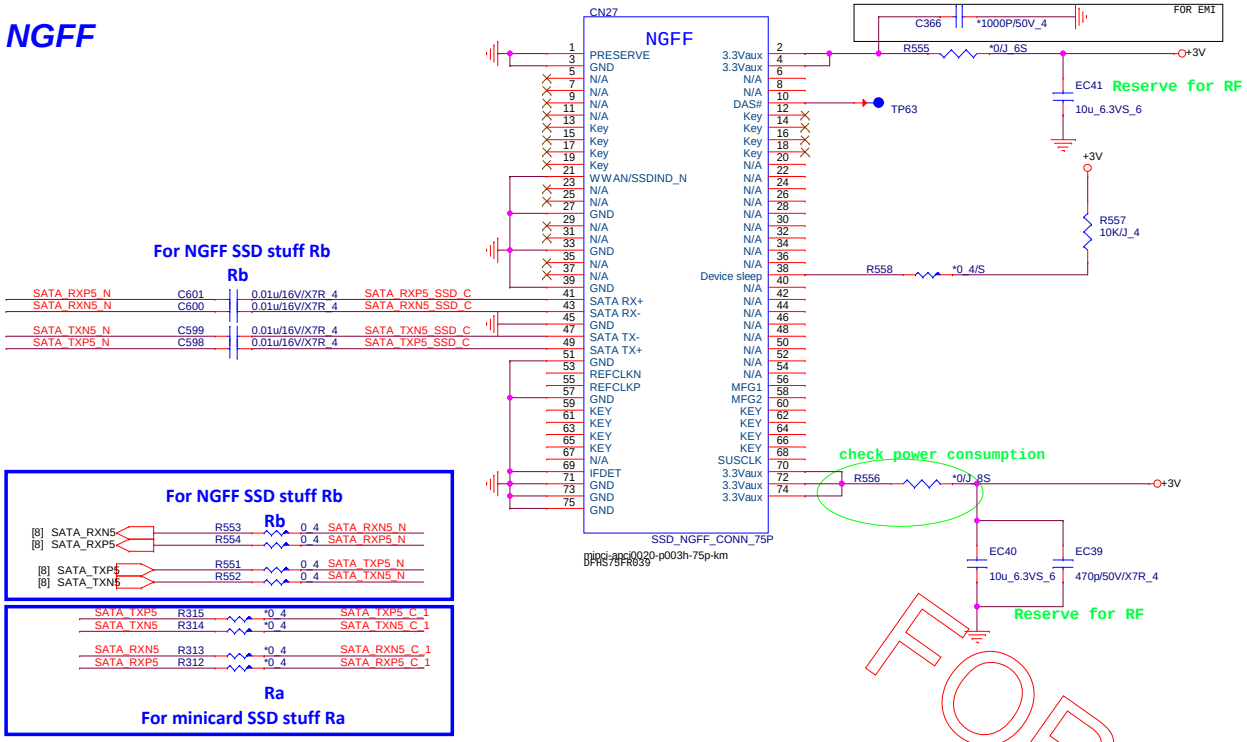
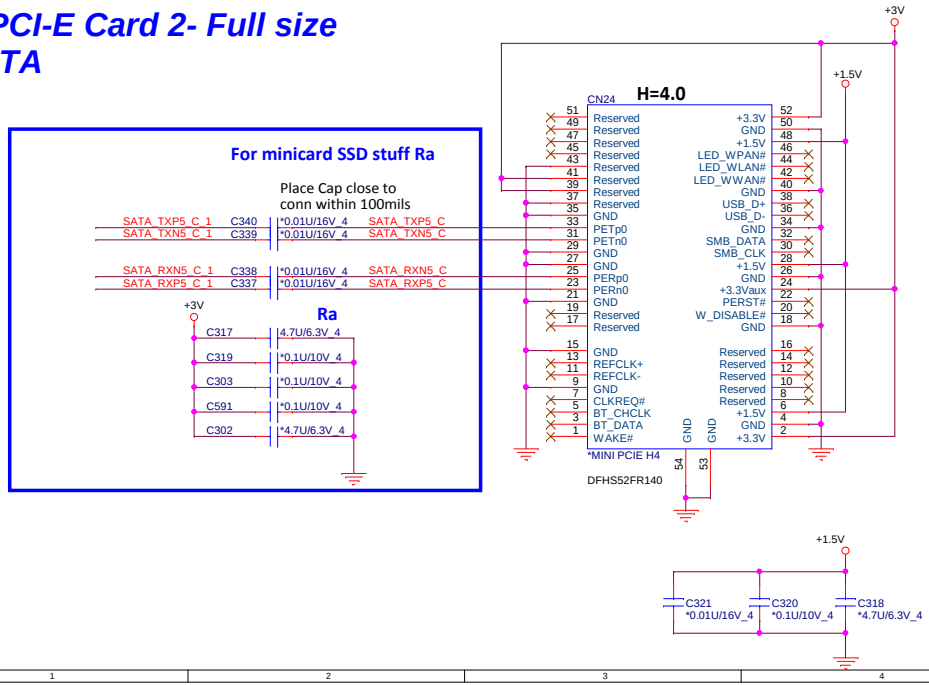
NGFF



pin	Type	Description
1	PRESENCE	This pin is grounded on the SSD. May be used by host to determine if slot is empty or populated
10	DAS#	Device Activity Signal
21	WWAN/SSDIND_N	This pin connect to Ground
38	Device Sleep Signal	If system didn't support DEVSLP, set DEVSLP Sleep Signal pin power high and keep (from power on), device will ignore. If system support DEVSLP, set DEVSLP Sleep Signal pin power low (from power on) device, device will support DEVSLP function. Device Sleep Signal H: SSD enter sleep model. Device Sleep Signal L: SSD exit sleep model.
53	REFCLKN	no connect on SSD
55	REFCLKP	no connect on SSD
56	MFG1	Manufacturing pin. Use determined by vendor. Must be a noconnect on the host board
58	MFG2	Manufacturing pin. Use determined by vendor. Must be a noconnect on the host board
68	SUSCLK	no connect on SSD
69	IFDET	This pin connect to Ground

FOR SW

Mini PCI-E Card 2- Full size mSATA



[2,7,8,9,10,11,13,14,15,16,17,18,19,20,21,22,23,24,26,27,32,34] +3V
[17,18,19,22,23,24,26,34] +5V
[18,24,29,30,31,32,33,34] +5VS5

NB5

PROJECT : Y19C
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NGFF/SSD	2A

Date: Wednesday, February 19, 2014 Sheet 25 of 34

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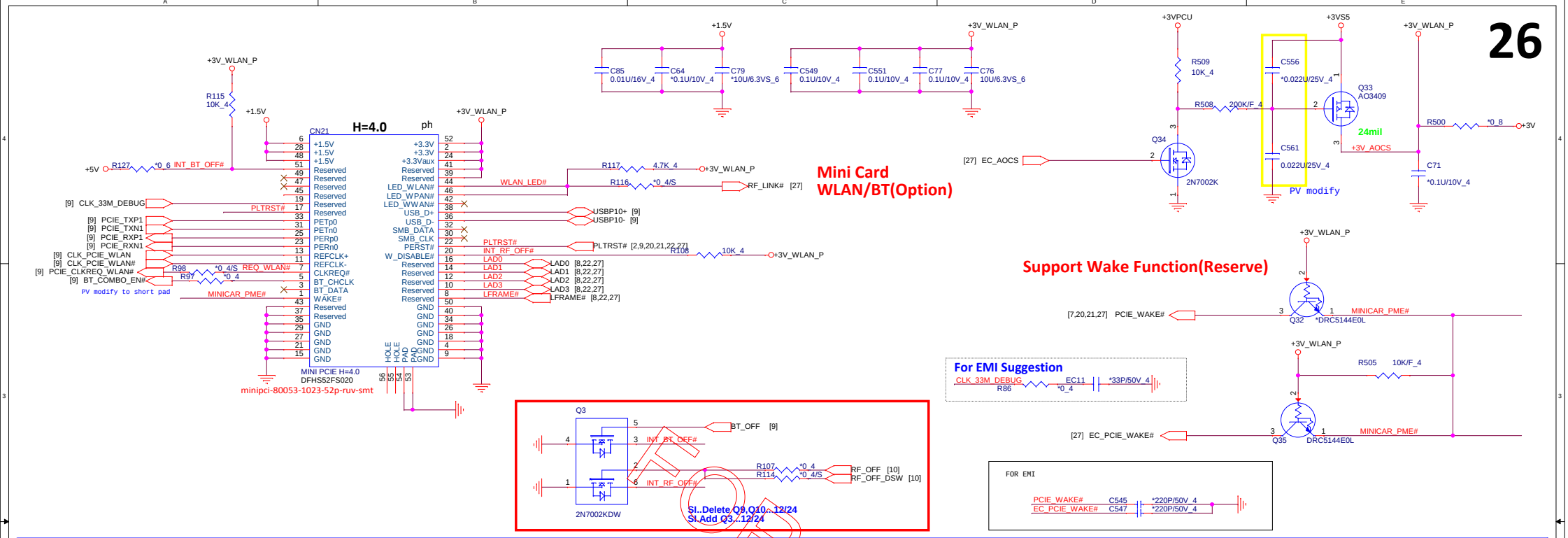
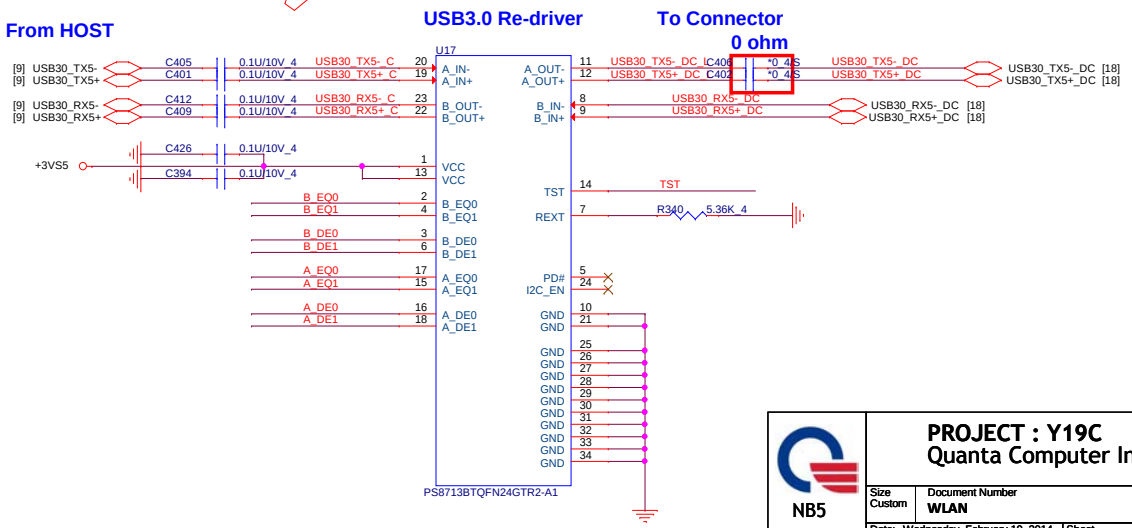


USB 3.0 re-driver

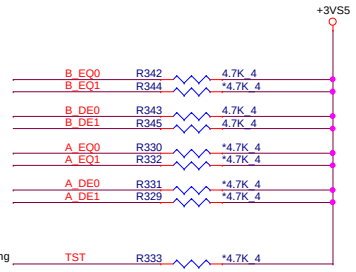


AEQ 9.5db / ADE 3.5db

BEQ 13db / BDE 5db / REXT 5.36K

A_EQ1 B_EQ1	A_EQ0 B_EQ0		A_DE1 B_DE1	A_DE0 B_DE0	
0	0	9.5dB	0	0	3.5dB
0	1	13dB	0	1	no de-emphasis
1	0	4.5dB	1	0	2.7dB
1	1	7.5dB	1	1	5dB

TST : Low = Normal LFPS swing / Hight =Turn down LFPS swing



PROJECT : Y19C Quanta Computer Inc.		
NB5	Size Custom / Document Number WLAN	Rev 2A
	Date: Wednesday, February 19, 2014 / Sheet 26of 34	

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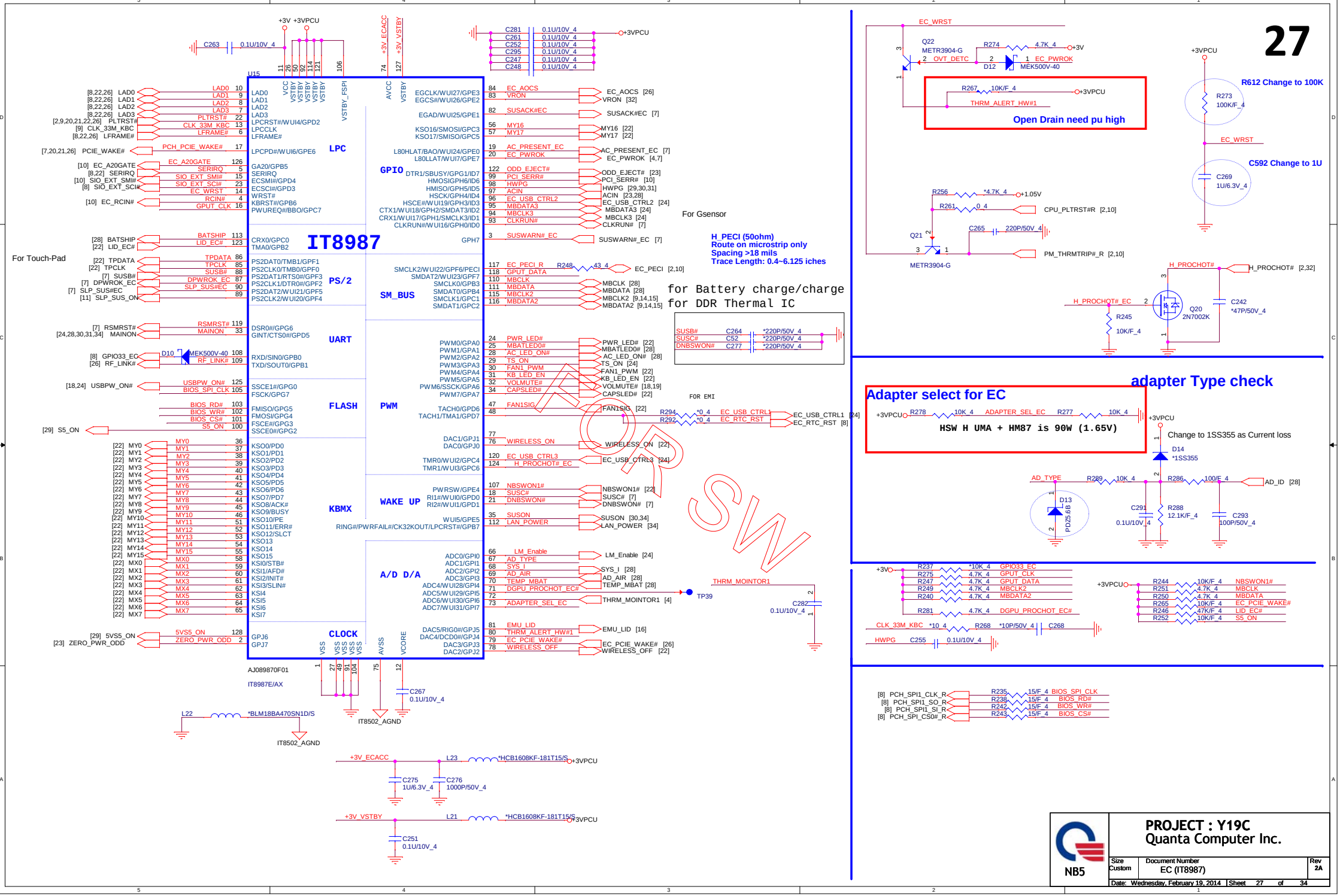
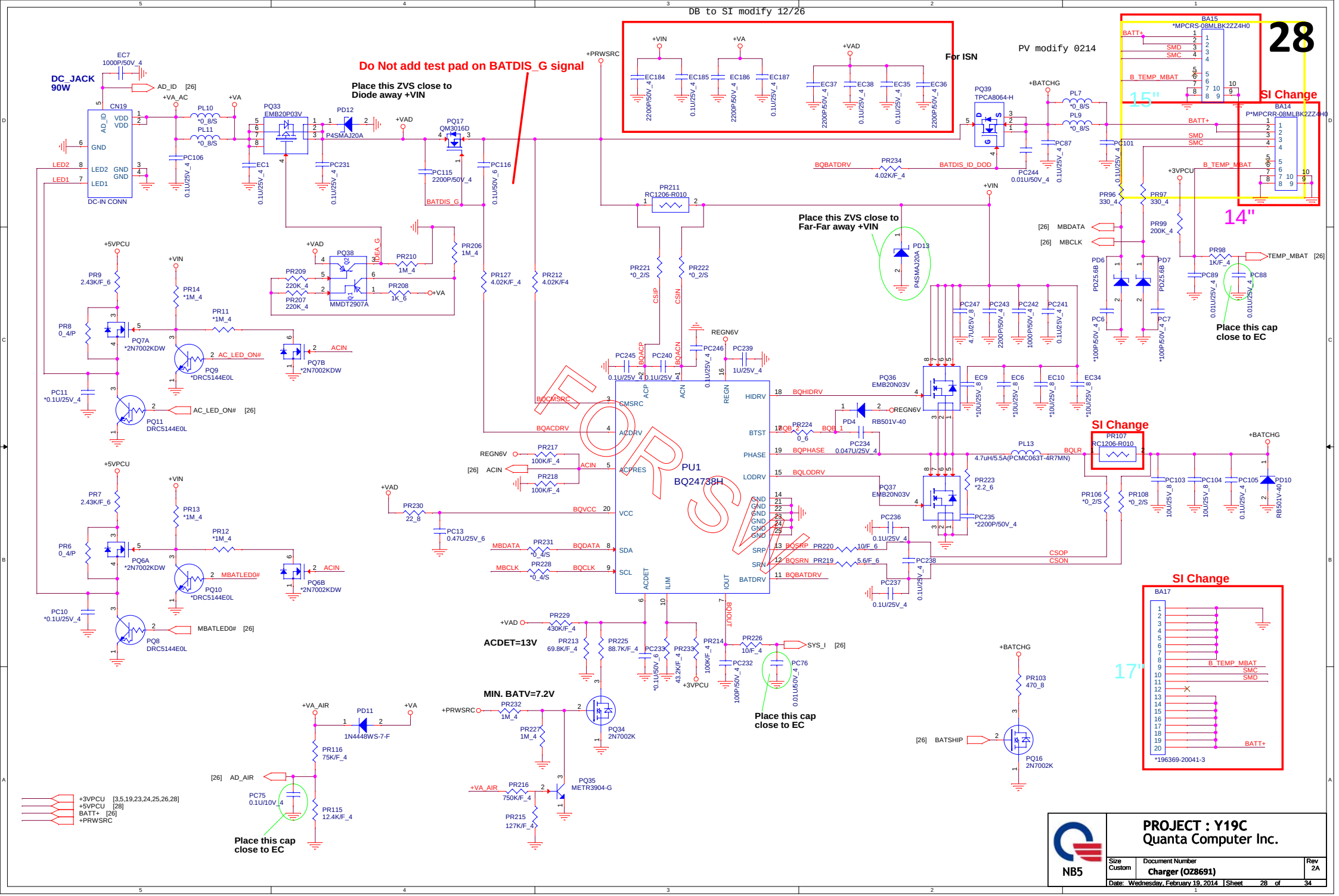
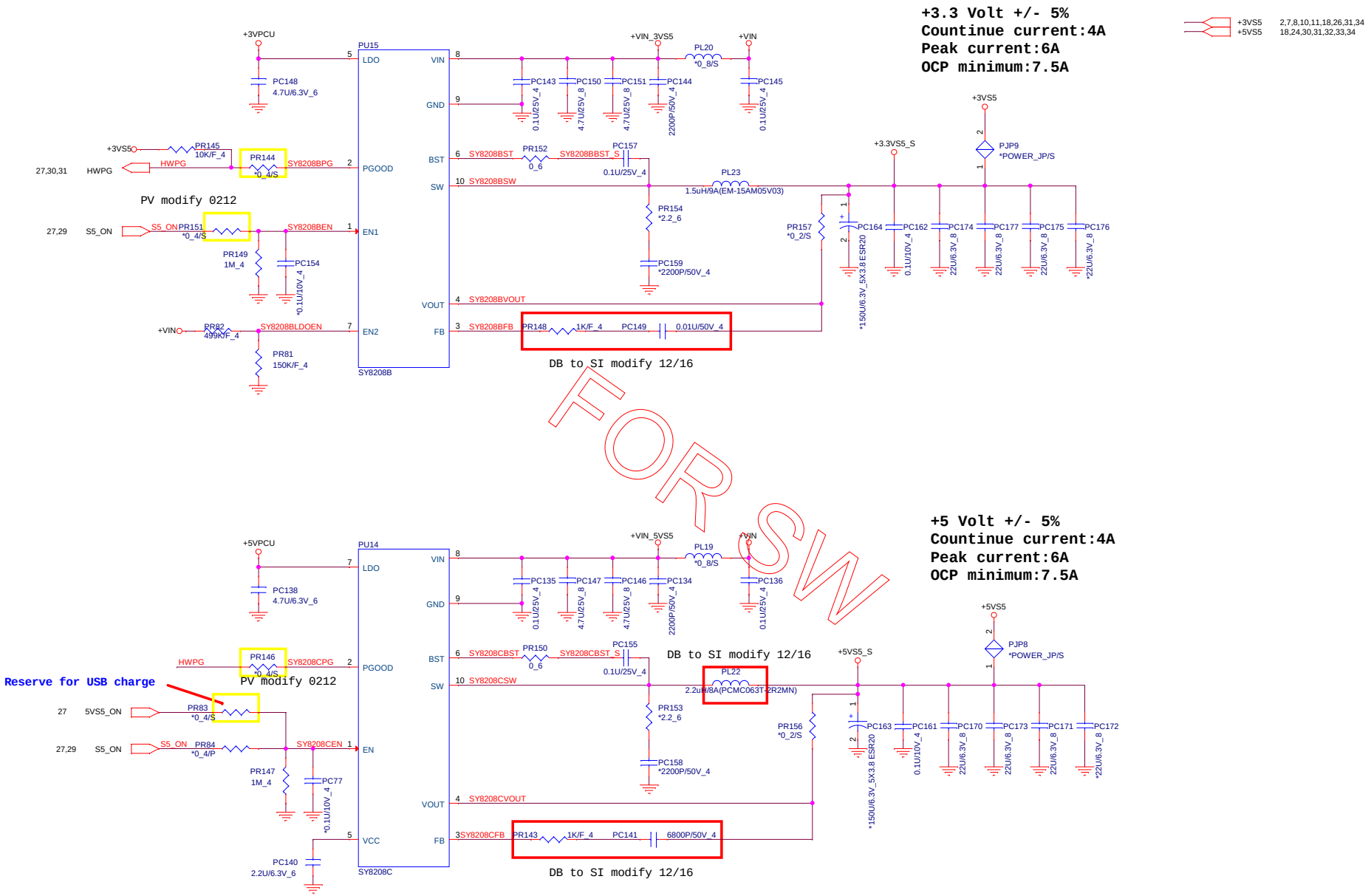


WWW.AliSaler.Com



WWW.AliSaler.Com



NB5	PROJECT : Y19C Quanta Computer Inc.	
Size Custom	Document Number 3/5VPCU(SY8208BC)	Rev 2A
Date:Wednesday, February 19, 2014	Sheet 29 of 34	

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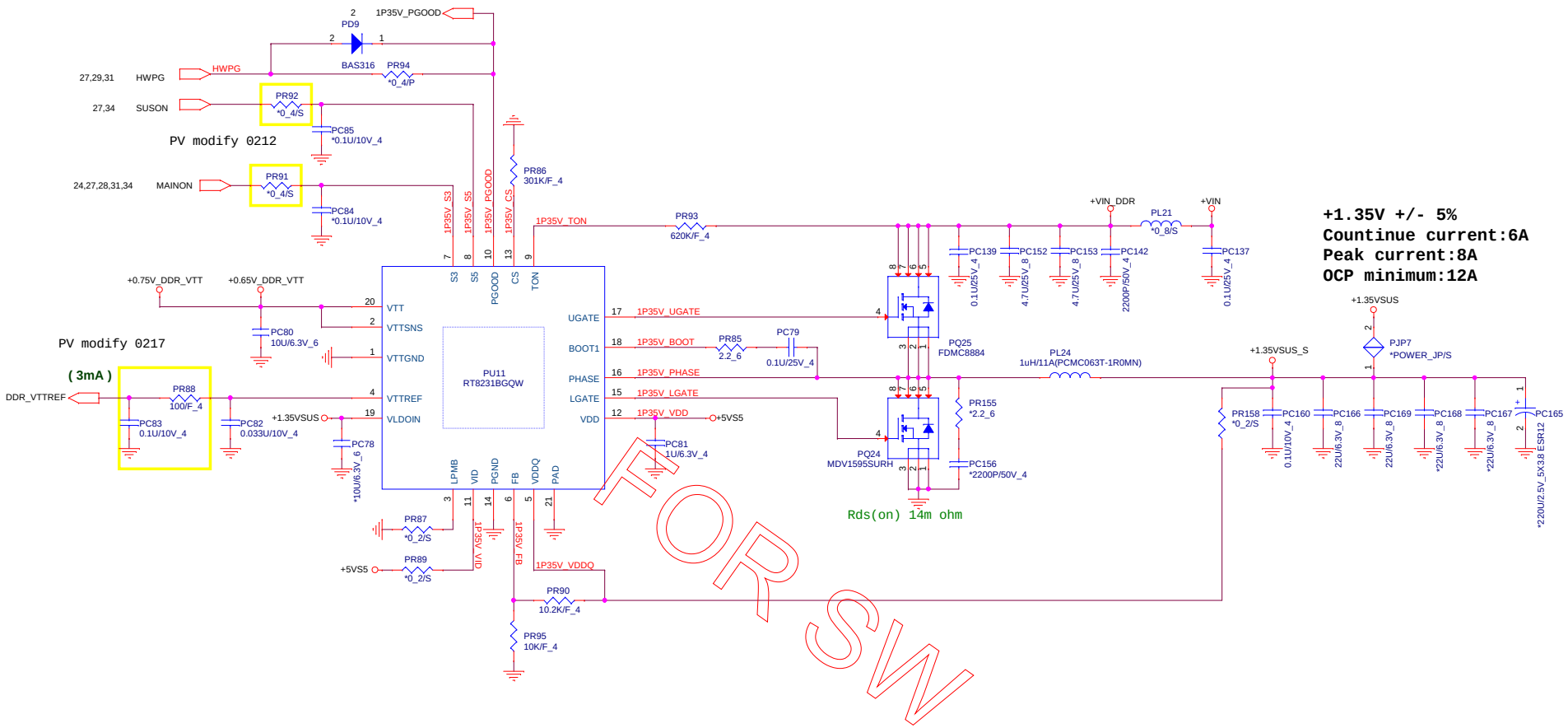

NB5	PROJECT : Y19C Quanta Computer Inc.	
Size Custom	Document Number DDR3 (RT8231A)/1.8VS5	Rev 2A
Date: Wednesday, February 19, 2014	Sheet 30 of 34	

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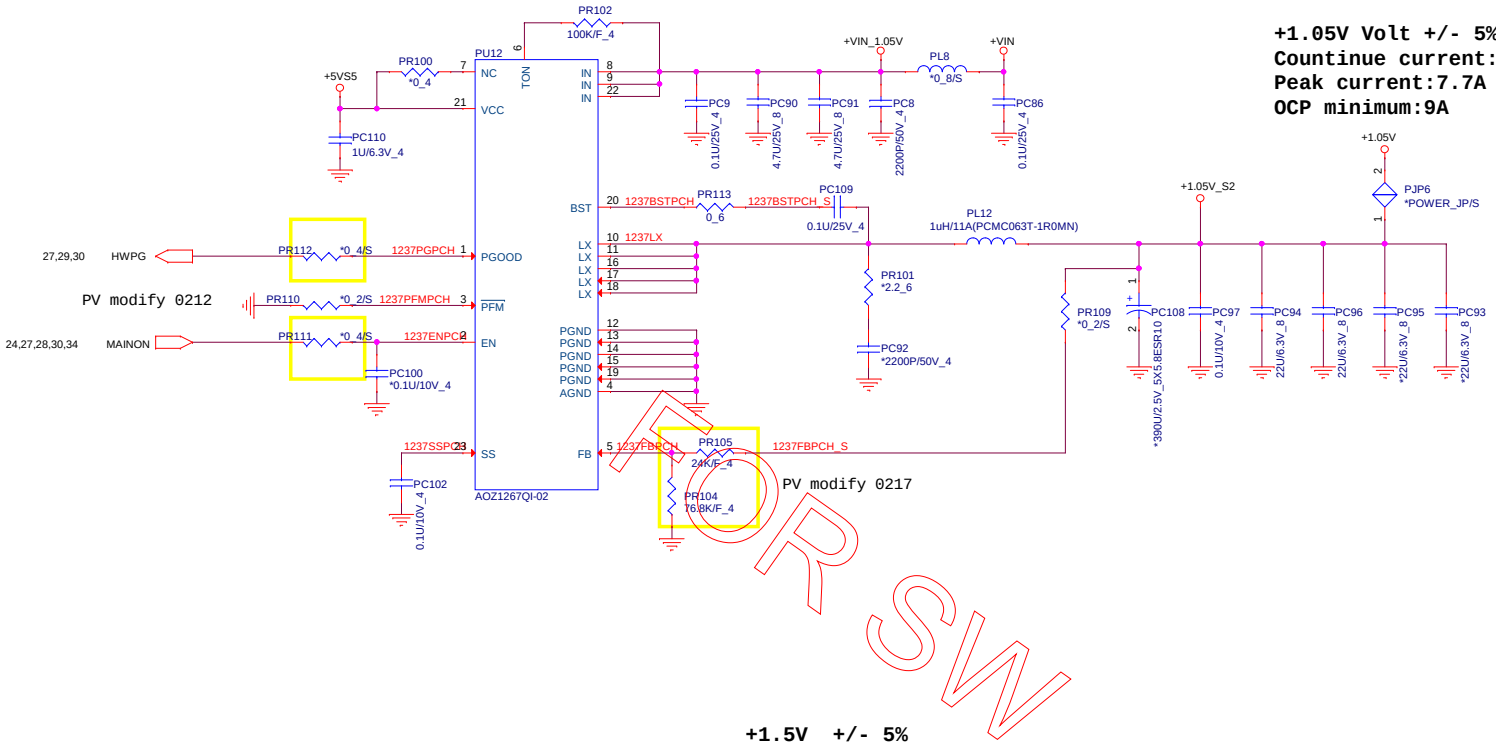

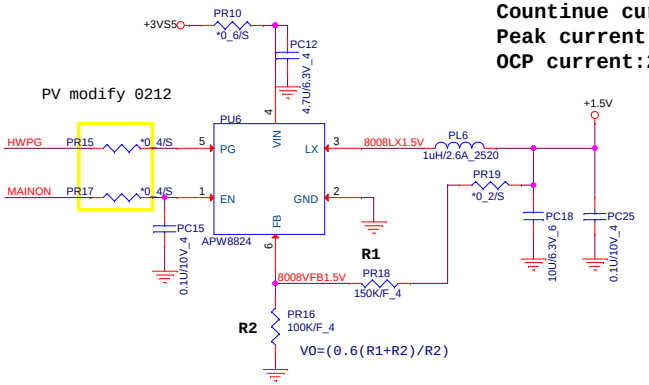

+VIN	16,19,22,23,28,29,30,32,34
+3VS5	2,7,8,10,11,18,26,29,34
+5VS5	18,24,29,30,32,33,34

PROJECT : Y19C
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	+1.1VS5 (RT8228)/2.5V	2A

Date: Wednesday, February 19, 2014 | Sheet 31 of 34

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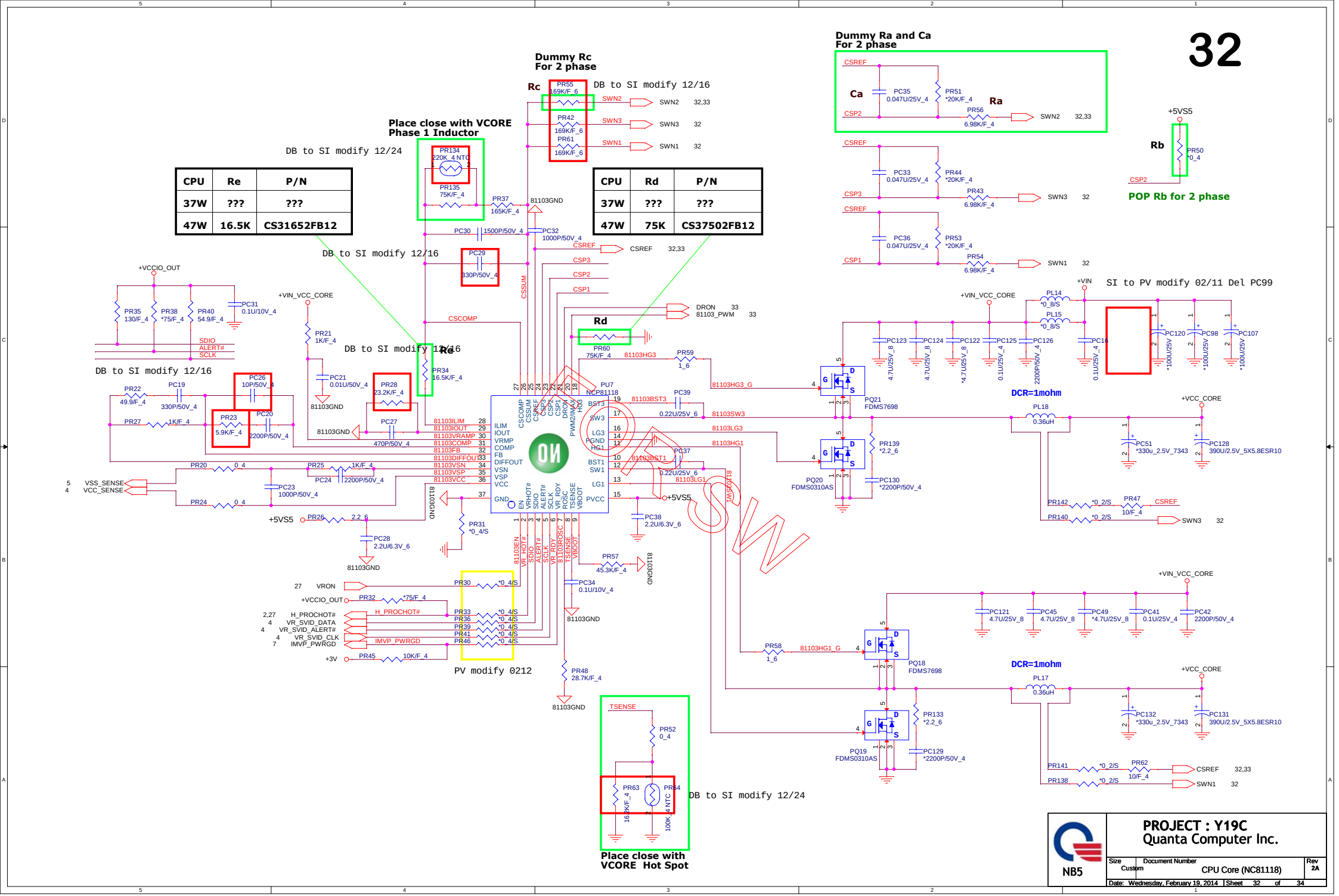

CPU	Re	P/N
37W	???	???
47W	16.5K	CS31652FB12

CPU	Rd	P/N
37W	???	???
47W	75K	CS37502FB12

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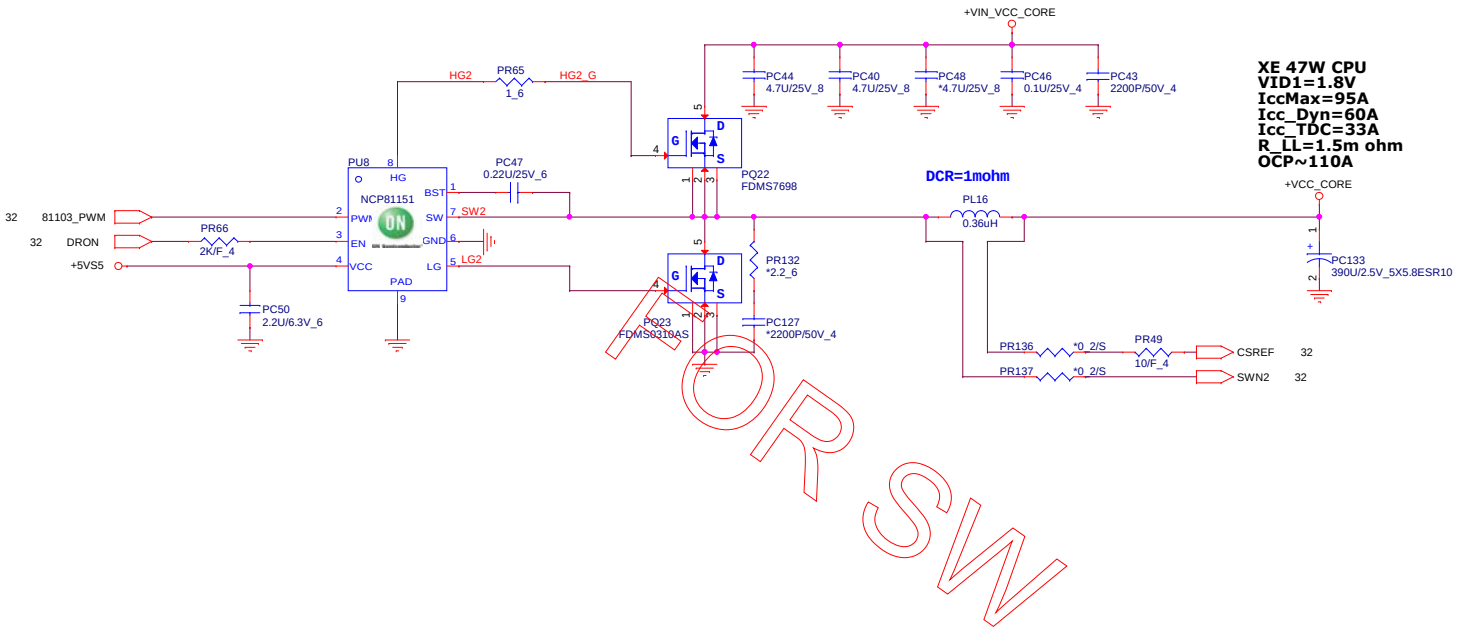

XE 47W CPU
VID1=1.8V
IccMax=95A
Icc_Dyn=60A
Icc_TDC=33A
R_LL=1.5m ohm
OCP~110A

FOR SW

+VCC_CORE 4,5,6,32

NB5

PROJECT : Y19C
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU Core2 (NCP81151)QC	2A

Date: Wednesday, February 19, 2014 | Sheet 33 of 34

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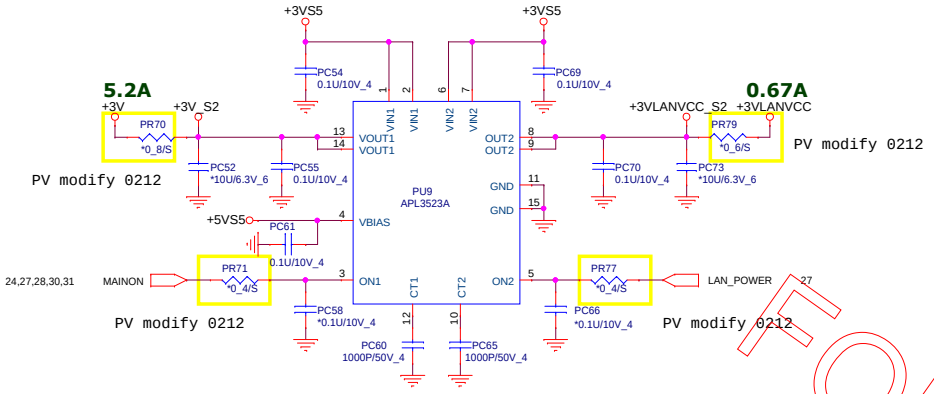

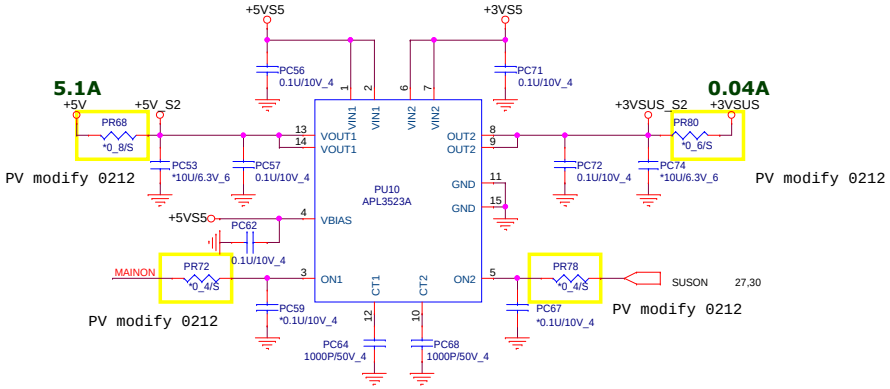

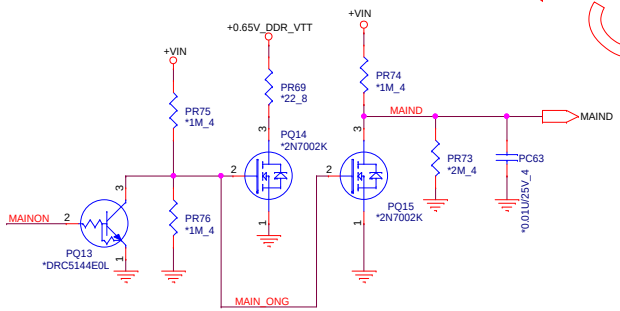

2,7,8,9,10,11,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27,32 +3V
17,18,19,22,23,24,26 +5V
16,19,22,23,28,29,30,31,32 +VIN
2,7,8,10,11,18,26,29,31 +3VS5
18,24,29,30,31,32,33 +5VS5
20,24 +3VLANVCC
13,14,30 +0.75V_DDR_VTT

NB5	**PROJECT : Y19C** Quanta Computer Inc.	
Size Custom	Document Number **Dis-charge IC (SLG55448)**	Rev 2A
Date: Wednesday, February 19, 2014	Sheet 34 of 34	

FOR SW

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